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(U) What's Beyond Moore's Law: Emerging Research Materials

ST Elbert

May 2009

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Pacific Northwest National Laboratory
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(U) Executive Summary

(U) Scope

(U) This report presents a technical assessment and forecast in the area "What's Beyond Moore's Law." The focus is on emerging research materials and how they may contribute to sustaining Moore's Law as conventional Complementary Metal-Oxide Semiconductor (CMOS) technology slows its traditional exponential growth that has supported Moore's Law for nearly two decades. The source of the problems CMOS is facing forms a background for the new materials that offer potential solutions. A contributing factor in the success of Moore's Law had been the semiconductor industry's ability to pattern ever smaller devices using continually refined lithographic processes. This report looks at the anticipated capabilities of the lithography in the context of the advanced materials that will be needed to pattern devices below 20 nanometers. A critical element of developing new materials is the ability to model and simulate their behavior, so the report covers this aspect as well.

(U) Objective

(U) The objective of this report is to produce a technical forecast of the sustainability of Moore's Law out to 2030 and beyond, within a framework of three time horizons: near-term (out to three years); mid-term (out to four to six years); and far-term (out to eight years and beyond). The report includes information on regional/geographic differences, breakthroughs, research and development investments, and signposts and indicators.

(U) Source of Data

(U) The primary source of data for this technical assessment and forecast has been an extensive literature review of advances in nanomaterials, nanodevices, and nanoelectronics. The progress being made has been set against the background of the International Technology Roadmap for Semiconductors (ITRS), which produced its last full report in 2007. A minor update in 2008 provides little new information. Nearly all of the information cited is available online, although access to the full papers is sometimes limited by subscription. The Hanford Technical Library was a valuable resource, with subscription access to nearly every source used in this report. The author's 30 years of research and experience in the fields of computational chemistry and materials science and high-performance computing was the basis of the judgment of the significance of the many thousands of research papers that were searched. The author would also like to thank his friends and colleagues, and in particular his wife, Vanda, for calling his attention to articles that he occasionally overlooked.

(U) Methodology

(U) The methodology used to prepare this report was broken down into three major topics and is reflected in the structure of this report:

1. **Background:** The background for this report is based on the scope and objective described above. It covers the underlying factors that have historically supported Moore's Law, including Dennard scaling and lithography. The current, near- and mid-term capabilities of deep and extreme ultraviolet

lithography are examined and then some of the barriers and challenges of future technologies are considered, including X-ray beams, electron beams, imprints, self assembly, metamaterial-based superlenses, and nonlinear optics. Recent advances and trends in emerging research materials are presented in the context of the ITRS report, with sections on low-dimensional materials (graphene, carbon nanotubes, and nanowires), macromolecules, directed self assembly, spin materials, interfaces and heterointerfaces, and finally modeling and simulation.

2. **Drivers/Factors/Scenarios:** There is intense competition to continue Moore's Law, driven by economics as much as technology. Three scenarios are presented describing how current trends might play out through the forecast period. The first is the displacement of silicon technology with carbon-based nanoelectronics. The second assumes that complex metal oxides play an expanded role in improving device scalability and functionality. Finally, the report considers the scenario where silicon maintains its dominant role and the growth of Moore's Law steadily declines.
3. **Technical Forecast:** Combining all the information in the previous sections, technical forecasts are produced in the context of the three scenarios.
   - **Near-term:** The next three years for the semiconductor industry are pretty well determined and the manufacturing capabilities are in the process of being refined and deployed. Performance improvements from logic devices will come from more cores per chip, not faster cores. A split between logic fabs and memory fabs may begin to emerge. The characterization of all the emerging materials will continue with the continued development of laboratory scale devices.
   - **Mid-term:** This is a critical period for the semiconductor industry as CMOS reaches the end of its ability to sustain Moore's Law but none of the emerging materials have reached sufficient maturity to take over. Integrated optical-electronic products offer the only hope of significant performance improvements by reducing bandwidth bottlenecks. The appearance of much higher frequency (>100 GHz) graphene-based transistors in the laboratory and the appearance of more complex devices will presage the return to the traditional growth of Moore's Law.
   - **Far-term:** Replacements for CMOS are at least ten years, and probably fifteen or more years away, but when they finally appear there is an excellent chance that they will put the industry back on the historic growth curve for Moore's Law, even for single core performance. There is a reasonable expectation that by 2030, single core performance will be in the teraherz range, with nanoscale patterning in the 1-10 trillion transistors per chip range. After that, vertical integration should support the traditional doubling of the number of transistors every two years past 2050.

(U) The report also provides an analysis of commercial adoption and implementation and a summary of research activities. The National Nanotechnology Initiative has been a major driver of recent work on emerging materials and it is important that it continue.

(U) Conclusions

(U) Carbon-based nanoelectronics provides perhaps the only real hope of displacing silicon in the semiconductor industry. It offers unparalleled capabilities for working in the quantum world at the nanoscale: ballistic electrons, optical coupling, quantum confinement, spin control, superior thermal and mechanical capabilities; and all at room temperature while being reasonably compatible with conventional fabrication processes. At the same time there is much that is not fully understood, such as

the Mott effect, and much to be learned about effective manufacturing processes. For such a new material, less than five years old, graphene has captured the imaginations of creative physicists and materials scientists everywhere—partly because it is relatively easy to work with. This makes support such as the National Nanoscale Initiative very important to maintain American leadership in this critical field. This all bodes well for a future bases on carbon where Moore's Law continues without fundamental physical roadblocks for several more decades.

(U) Predicting the replacement of silicon is not something to be taken lightly. Silicon has served the semiconductor industry exceptionally well for over fifty years. The financial investments of the industry in silicon are formidable and it will not yield its preeminent position easily. At the same time, carbon offers unquestionable competitive advantages—if they can be delivered competitively. It may be possible to mass produce carbon-based chips without going to the nanoscale, but at the nanoscale, expect carbon to surpass silicon.

(U) Abbreviations, Acronyms, and Terms

(U) **AFM**	Atomic force microscope; a very high-resolution type of scanning probe microscope with resolutions of fractions of a nanometer.
(U) **AMD**	Advanced Micro Devices, Inc.
(U) **ASIC**	Application-Specific Integrated Circuit: an integrated circuit (logic device) customized for a particular use that cannot be altered after manufacturing.
(U) **BCP**	Block copolymers; two chemically dissimilar polymers linked by covalent bonds.
(U) **BMG**	Bulk metallic glass; an amorphous metal, *i.e.*, one with a disordered, non-crystalline atomic-scale structure, with a low critical cooling rate that allows the formation of amorphous structure in thick layers (over 1 mm).
(U) **Chirality**	a property of asymmetry or "handedness".
(U) **CMOS**	Complimentary Metal-Oxide Semiconductor; the most common modern integrated circuit manufacturing process.
(U) **CMR**	Colossal magnetoresistance; a property of some materials that enables them to dramatically change by orders of magnitude their electrical resistance in the presence of a magnetic field.
(U) **CNT**	Carbon nanotube
(U) **CVD**	Chemical vapor deposition; the process used by the semiconductor industry to produce thin films by exposing a substrate (wafer) to one or more volatile chemicals that are deposited on the surface.
(U) **DRAM**	Dynamic Random Access Memory; a dense, slow, volatile semiconductor memory that stores each bit of data using only one capacitor and one transistor. Since the capacitors leak charge, they must be refreshed dynamically.
(U) **Deep UV**	Deep ultraviolet; the ultraviolet spectrum between 120 nm and 300 nm.
(U) **ERD**	Emerging Research Devices
(U) **ERM**	Emerging Research Materials
(U) **EUV**	Extreme ultraviolet; the short wavelength section of the ultraviolet spectrum, generally considered to span the region from 10 nm to 120 nm.
(U) **fab**	Short for semiconductor fabrication plant, where integrated circuit devices are manufactured.
(U) **FEP**	Front End Processes; wafer fabrication process technologies and materials.
(U) **FET**	Field-effect transistor; a type of transistor that relies on an electric field to control the conductivity of a channel for a charge carrier (electrons, n-type, or holes, p-type) in a semiconductor material.

(U) **FPGA**	Field Programmable Gate Array; a logic device that can be configured after manufacturing.
(U) **Gb**	Gigabits; 10^9 bits (not bytes). Gigabytes would be abbreviated GB.
(U) **GHz**	Gigahertz; one billion (10^9) cycles per second.
(U) **GMR**	Giant magnetoresistance; a quantum effect observed in thin film structures that manifests itself as a significant decrease (10-80%) in electrical resistance in the presence of a magnetic field.
(U) **GNR**	Graphene nanoribbon
(U) **HMOS**	High-performance Metal Oxide Semiconductor; a digital circuit style that uses n-type MOSFETs to implement logic gates. A type of depletion-load n-channel MOS superseded by CMOS in the early 1980s.
(U) **IBM**	International Business Machines, Inc.
(U) **IRC**	International Roadmap Committee
(U) **ITRS**	International Technology Roadmap for Semiconductors
(U) **MC68000**	A 16/32-bit microprocessor using 3.5 micrometer HMOS technology introduced in 1979 by Motorola (now Freescale).
(U) **MD**	Molecular dynamics; a form of simulation where atoms and molecules are allowed to interact for a period of time using approximations of the physical forces involved.
(U) **Metamaterial**	A material that gains its properties from its structure rather than directly.from its composition.
(U) **MHz**	Megahertz; one million (10^6) cycles per second.
(U) **MIT**	Massachusetts Institute of Technology
(U) **mm**	millimeter; one thousandth (10^{-3}) of a meter.
(U) **µm**	micrometer; one millionth (10^{-6}) of a meter.
(U) **MOS**	Metal-oxide-semiconductor; a material traditionally obtained by growing a layer of silicon dioxide (SiO_2) on top of a silicon substrate and covering with a layer of metal or polycrystalline silicon.
(U) **MOSFET**	Metal-oxide-semiconductor field effect transistor.
(U) **MRAM**	Magnetoresistive random access memory; a nonvolatile memory that stores information magnetically, using a variety of approaches.

(U) **n-type**	a semiconductor or transistor where the charge carriers are negative, *i.e.*, electrons.
(U) **NDR**	Negative Differential Resistance; a property of circuit elements in which, over certain voltage ranges, current is a decreasing function of voltage rather than increasing.
(U) **NEC**	NEC Corporation; Nippon Electric Company Limited before 1983.
(U) **NIL**	Nanoimprint lithography; a method of fabricating nanometer scale patterns by mechanical deformation.
(U) **NIST**	National Institute of Standards and Technology, an agency of the U.S. Department of Commerce. Known as the National Bureau of Standards (NBS) until 1988.
(U) **nm**	nanometer; one billionth (10^{-9}) of a meter.
(U) **NRAM**	nano-random access memory; a nonvolatile memory based on the mechanical position of carbon nanotubes.
(U) **p-type**	a semiconductor or transistor where the charge carriers are positive, *i.e.*, holes.
(U) **PCM**	Phase-change memory; also called PRAM
(U) **PCRAM**	Phase-change random access memory; also called PRAM
(U) **PDA**	Personal digital assistant; a handheld computer.
(U) **PMC**	Programmable metallization cell memory; a non-volatile memory based on the physical relocation of ions within a solid electrolyte. Also called conductive-bridging RAM or CBRAM.
(U) **PRAM**	Phase-change random access memory; single-bit addressable non-volatile memory that uses the unique behavior of chalcogenide glass, which has two states, crystalline and amorphous, that can be changed by heating.
(U) **RRAM**	Resistive random access memory; a non-volatile memory using various dielectric materials.
(U) **Semiconductor**	A material with a conductivity value between that of a conductor and an insulator and the conductivity can be varied under the control of an external electrical field.
(U) **SPCM**	Scanning photocurrent microscopy
(U) **SRAM**	Static random access memory; a fast, volatile semiconductor memory using six transistors compared to one for DRAM
(U) **SWCNT**	Single-walled carbon nanotube; a carbon nanotube with only one layer of carbon.
(U) **SWNT**	Single-walled (carbon) nanotube.

(U) **THz**	Teraherz; one trillion (10^{12}) cycles per second.
(U) **TMR**	Tunnel magnetoresistance; a quantum effect that occurs in magnetic tunnel junctions where electrons are more likely to tunnel through the insulating film when the surrounding ferromagnetic films are oriented in parallel than antiparallel.
(U) **TTL**	Transistor-transistor logic; a class of digital circuits built from bipolar junction transistors that consume substantially more power than equivalent CMOS devices.
(U) **USB**	Universal Serial Bus; a serial bus standard used to connect devices to a host computer.
(U) **UV**	ultraviolet; the portion of the electromagnetic spectrum with a wavelength shorter than visible light but longer than x-rays, *i.e.*, in the range 10 nm to 400 nm.

(U) Contents

(U) Figures

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1.0 (U) Introduction

1.1 (U) Purpose and Objective

(U) The objective of this report is to provide a technical assessment and forecast in response to the topic "What's Beyond Moore's Law?" For over forty years Moore's Law has held up, but today's leading-edge chips contain features only 100 atoms long. As the technology approaches atomic limits, what happens next? Will the exponential growth characteristic of Moore's Law slow and eventually halt? What form will growth take? Nanowires? New materials? Vertical integration?

(U) Several industry roadmaps foresee an end to Moore's Law around 2018-2020 with current technologies. This report primarily focuses on the premise that assumes Moore's Law continues beyond 2020 and will attempts to answer the following questions:

- What are the most likely technologies to be employed?
- What are the fundamental obstacles that will have to be defeated or finessed?
- Will power requirements continue to climb?

(U) In the case Moore's Law does slow or stall, the report considers the following questions:

- What are the technological implications?
- Will the performance gap between FPGA and ASIC designs narrow or remain static?
- Are there technologies such as storage density where Moore's Law continues despite minimal improvements in transistor density?

1.2 (U) Outline of this Report

(U) This technical assessment and forecast report is presented in the following sections:

- **Background**: This section provides a review of the relevant background on the current state of Moore's Law, the challenges that threaten its continuation, and the technologies that may contribute to sustaining future growth.
- **Scenarios**: This section postulates two scenarios where the growth of Moore's Law is sustained and one in which it is not.
- **Technical Forecast**: This section combines the research directions outlined in the Background section with the scenarios to cover anticipated outcomes for the three time horizons: near-, mid-, and far-term. The near-term is out to three years, the mid-term is out to six years, and the far-term is out to eight years and beyond.
- **Commercial Adoption/Implementation** : This section reviews the economic forces influencing the technology and the how the technology is likely to influence the semiconductor industry.
- **Research Activities**: This section discusses the ongoing worldwide technical advances and how they will impact the technology.
- **Conclusions**: This section summarizes the essence of the forecast and its implications for the NSA

2.0 (U) Background

2.1 (U) Moore's Law

(U) In 1965 Gordon Moore[1] recognized that integrated circuit components were steadily becoming more cost-effective through a series of technology shifts. Using just four data points from the years 1962 to 1965, he predicted that the number of components in an integrated circuit would double every year for at least ten years and that by 1975 "the number of components per integrated circuit for minimum cost will be 65,000." When Moore revisited the issue of exponential growth in 1975,[2] he noted that there did indeed exist a 16 kilobit charge-coupled device memory chip with about that many transistors, but he lowered the slope of the growth curve to a doubling period of every two years because circuit cleverness had run out of ideas, i.e., device layout had reached its optimal density. Transistor density in processor chips is typically less than in memory chips, due to lower device regularity, so it wasn't until 1979 that Motorola introduced a comparably dense processor in the 32-bit MC68000 with 68,000 transistors. It used 4 µm HMOS technology (a high density n-channel MOS predecessor of CMOS) with a clock frequency of 8 MHz and a power requirement of 1.2 watts. The exponential growth in the number of components on a single integrated circuit has continued unabated. As shown in Figure 2.1, using data on processor chips from 1971 (Intel 4004, 2K transistors) to 2008 (IBM z10, 993M transistors), the trend is remarkably consistent despite the technology shifts that place points above and below the trend line. Projecting the trend backwards gives 1950 as the year with one transistor. Although the transistor was invented in 1947, *Fortune* magazine waited until 1953 to designate "The Year of the Transistor" and the first planar transistor did not appear until 1959. Looking to the future, the figure shows about 46 billion transistors per chip in 2020 and 1.5 trillion transistors in 2030—if the trend continues. The end of the trend has been predicted many times, but so far a series of different technologies, all using silicon and its oxide, have managed to maintain the overall trend. How and whether the trend continues (or not) is the subject of this forecast. Moore's Law will clearly end at some point. The end of CMOS may not be far off,[3] but basic physical limits have been used to estimate that the maximum lifetime is 600 years.[4] More immediately, however, it is first necessary to explore the elements that have made much of Moore's Law possible: Dennard scaling.

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[1] (U) Moore, G.E., "Cramming more components onto integrated circuits," *Electronics*, **38**(8), 114-117 (19 April 1965) [reprint doi:10.1109/JPROC.1998.658762]

[2] (U) Moore, G.E., "Progress in Digital Integrated Electronics," *Electron Devices Meeting, 1975 International*, **21**, 11-13 (1-3 December 1975) [available online]

[3] (U) Zhirnov, V.V., R.K. Cavin III, J.A. Hutchby, and G.I. Gourianoff, "Limits to binary logic switch scaling - a gedanken model," *Proceeding of the IEEE*, **91**(11), 1934-1939 (November 2003) [doi:10.1109/JPROC.2003.818324]

[4] (U) Krauss, L.M., G.D. Starkman, "Universal Limits on Comutation," arXiv:astro-ph/0404510v2 , (10 May 2004)

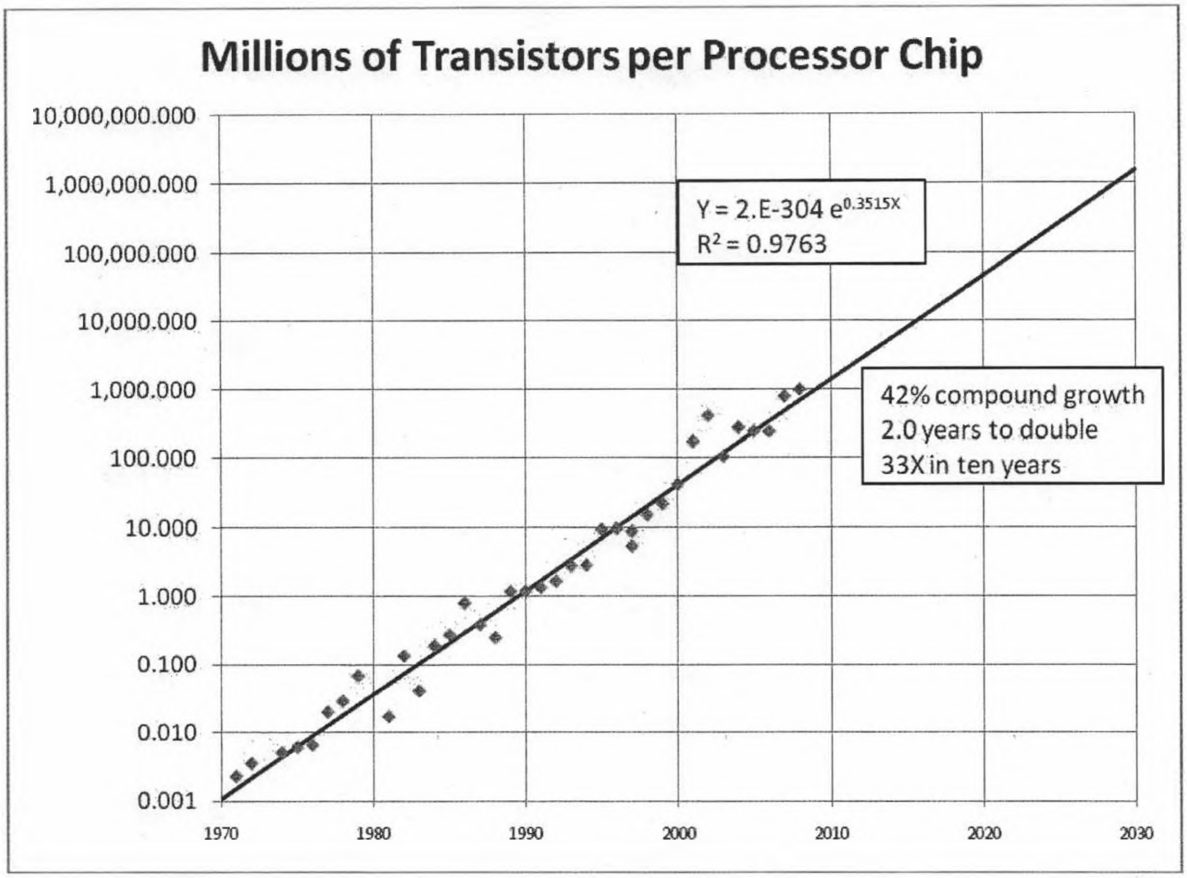

Figure 2.1. (U) Exponential growth of the number of transistors per processor chip

2.2 (U) Dennard Scaling

(U) In 1974 Robert Dennard, *et al.*[5] at IBM, explored the different methods of scaling MOS devices. The key observation was that if voltages were scaled with device dimensions, the devices became faster and used less energy. Furthermore, the energy reduction per device exactly matched the increase in energy resulting from being able to place more, smaller devices in the same area of the chip so the power per chip stayed constant. This means that with the right technology, scaling will work. The hard part is finding a way to make transistors smaller in a way that can be done practically with high volume manufacturing.

(U) For thirty years the semiconductor industry has succeeded in developing lithographic techniques to pattern smaller feature sizes, growing thinner gate oxides and reducing defect levels at increasingly challenging dimensions. To double the number of transistors in two years means the feature size needed to be reduced by one over the square root of two, i.e., 0.71, or by half every four years. The scaling that

[5] (U) Dennard, R.H., R.H. Gaenssien, V.L. Rideout, E. Bassous, and A.R. LeBlanc, "Design of ion-implanted MOSFETs with very small physical dimensions," *IEEE Journal of Solid State* Circuits, 9(5), 256-268 (October 1974) [available online]

Dennard foresaw did not really take place, however, until the shift to CMOS was nearly complete. The TTL logic that dominated processor fabrication before CMOS maintained a standard voltage level and outperformed CMOS at that scale while using other techniques, including increasing chip size, to increase the number of transistors per chip. Since CMOS was adopted the increase in the number of transistors has come through size scaling. Although there has been some variation in the introduction of new technologies, the overall trend has been remarkably consistent, as shown in Table 2.1, which shows the integration scale (feature size in nanometers) and the year a microprocessor using this technology was introduced. The late nineties actually saw accelerated shrinkage of gate lengths (although not gate pitch) in order to achieve higher performance, resulting in clock speeds of >3 GHz sooner than most experts had predicted. It is believed the 32 nm generation is approximately on schedule, but there are many questions about the next generation at 22 nm and the ones that follow. This is not so much a limitation of CMOS yet, but of the lithographic technology used to pattern the devices and is a challenge for any technologies that would replace CMOS as well.

Table 2.1. (U) CMOS device size scaling at ~0.7x every two years

Target Production	"Feature Size" in nm	Product Year	Company
1990	1,000	1989	Intel
1992	750	1991	DEC
1994	500	1994	IBM, Motorola, DEC
1996	350	1995	Intel
1998	250	1998	IBM, Fujitsu, MIPS, HP
2000	180	2000	IBM, Intel
2002	130	2000	Fujitsu
2004	90	2001	IBM
2006	65	2006	Intel
2008	45	2008	Intel
2010	32	(Q4 2009) (2013)	Intel (ITRS roadmap)
2012	22	(2016)	(ITRS roadmap)
2014	16	(2019)	(ITRS roadmap)
2016	11	(2022)	(ITRS roadmap)

(U) The ITRS roadmap, discussed in the next section, predicts the "feature size" rate of decrease began slowing after 2005 to a rate of 0.71X every 2.5 years and that a further slowing to every 3 years will take place after 2010 so the last three rows of Table 2.1 are very optimistic.

(U) The term "feature size," sometimes called node size, is in quotes because it means different things in different contexts. It used to mean the smallest parts of the transistors on the chips, commonly half the distance between the metal lines that power the transistor (half-pitch) as shown in Figure 2.2. Logic

devices (microprocessors) used to lag memory devices in half-pitch size by two or three years, but the drive to increase processor speeds in the late nineties drove the shrinkage of logic gate size so that by 2000 the logic gate had become the smallest feature produced by the semiconductor industry. The 65-nm Intel Core 2 processor available in 2006 has a gate length of 32 nm but a half-pitch for the first level of wires of 105 nm.[6] The roadmap shows 25 nm as the MPU physical gate length (smaller than the printed gate length) corresponding to a 65-nm DRAM half-pitch "feature size."

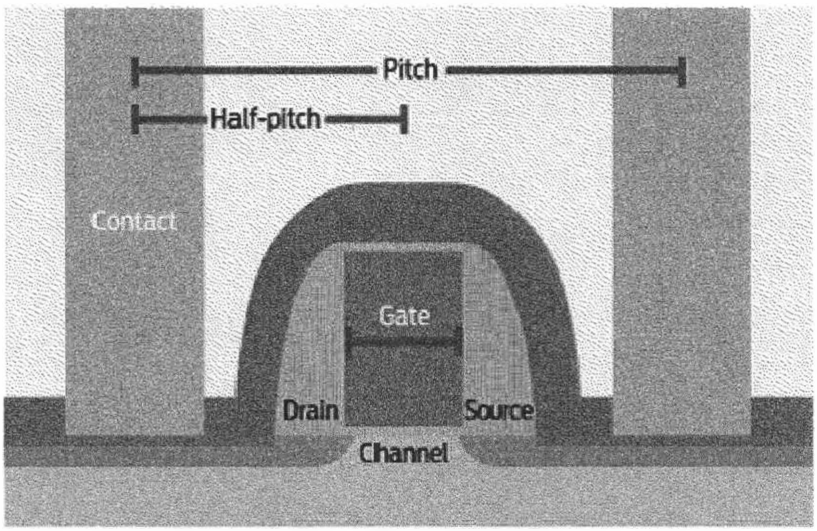

Figure 2.2. (U) "Feature Size" dilemma. The half-pitch of the first wiring layer is the defining feature for memory chips, while the gate length is key for logic chips. Neither is entirely representative of the "feature size." (from IEEE Spectrum, **45**, no. 4 (NA), April 2009, p. 28.)

(U) The 2007 roadmap expected 45 nm "feature size" products with a gate length of 18 nm to appear in 2010, but Intel began marketing the Core i7 as a 45-nm product in 2008. The roadmap shows 32 nm technology, with 13 nm logic gates, appearing in 2013 and 16 nm, with 6-nm logic gates in 2019. Today's cutting-edge pre-production "32-nm" logic chips are actually at a 50- or 56-nm *half-pitch* and the equivalent memory chip is at about a 34-nm half-pitch. Intel demonstrated a 32-nm test chip with 1.9 billion transistors and a cell size of 1.82 μm^2 at the September 2007 Intel Developer Forum.

2.3 (U) Lithography

(U) Despite the confusion of what dimension means what, the technology that enabled Dennard scaling and hence Moore's Law itself is the lithographic process. Conceptually similar to chemical photography, semiconductor devices are "developed" in a series of exposures to images projected by light through a series of masks onto the chip covered with photosensitive material. The process has become more sophisticated and complicated with each generation. Starting from 16-mm movie-camera lenses and visible light, the process now involves lenses that weigh nearly half a metric ton, cost several million

[6] (U) Arnold, B., "Shrinking Possibilities," *IEEE Spectrum*, **45**(4)(NA), 26-56 (April 2009) [online]

dollars and use light deep in the ultraviolet. Although lithography is not the focus of this report, it (or its successors) play a critical role in building manufacturable nanoscale devices so a brief survey is presented here as background information.

(U) Photon-based lithography is not the only possibility for getting to the nanoscale. Possible next generation technologies are electron beam lithography, imprint lithography, self-assembled structures, superlenses built with metamaterials, and imaging with nonlinear media. All but the first involve emerging research materials and significant computational design requirements. As will be seen, emerging research materials play a role.

2.3.1 (U) Deep Ultraviolet

(U) Deep ultraviolet lithography as currently practiced using 193-nm light from argon-fluoride lasers and high-index immersion is limited to 38-nm half-pitch. Immersing a lens with a high refractive index in a liquid (typically water) with a refractive index higher than air allows sharper images. This is sufficient for the current 45-nm generation. The semiconductor industry seems to be betting that tricks such as double-exposure patterning, will be able to produce sub-30 nm features and get to the 32-nm generation. In December 2008 Intel said it was on track to begin production using 32-nm process technology in the fourth quarter of 2009 using enhanced immersion and deep UV. Patterning features at less than one-sixth of a wavelength is a technological tour-de-force. Using higher-index immersion fluids and lenses was considered a promising technology, but is now in doubt as Nikon dropped its high-index 193-nm lithography equipment program.[7]

(U) How to get to 22-nm features is an open question. An effort to use 157-nm light failed when it was realized that the method needed more high-purity CaF_2 lens material than seemed achievable for high-volume manufacturing. Intel has stated it expects to begin production with 22-nm process technology using enhanced deep UV methods, but may then shift to extreme ultraviolet (EUV) light at 13.5 nm (see below). IBM, in a press release on 18 August 2008,[8] announced that it and its partners (AMD, Freescale, STMicroelectronics, Toshiba, and the College of Nanoscale Science and Engineering at SUNY-Albany) had develop the first working SRAM memory cell built on a traditional six-transistor design using 22-nm technology at the 300mm research facility in Albany.

(U) The deep UV enhancements being considered include phase-shift mask lithography using pixilated masks and computational lithography as well as optical proximity correction in addition to further refinements of strain technology and high-κ/metal gate technology, reduction of parasitic resistance and capacitance, multigate FETs, novel co-implants, advanced activation energy techniques, thin silicide and damascene copper contacts. In other words, while recognizing there are serious problems with optical lithography in the coming years, the resources being committed to solve these problems are considerable and there does not seem to be a shortage of clever ideas. As the world of optical computing has learned, never underestimate the capability of semiconductors.

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[7] (U) LaPedus, M., "Who killed high-index lithography?," *EE Times*, (27 May 2008) [online]
[8] (U) IBM press release: "IBM Builds World's Smallest SRAM Memory Cell," Yorktown Heights (18 August 2008) [online]

2.3.2 (U) Extreme Ultraviolet

(U) EUV light at 13.5 nm has a wavelength clearly capable of reaching nearly nanoscale resolution, but optical resolution may not be the limiting factor. Whether or not it takes over from deep UV at 22 nm, it seems to be the only optical lithographic technology capable of reaching 16 nm, which many expect to be the point where the electronics industry transitions from CMOS to nanoelectronics. All matter absorbs EUV, so producing a strong beam of focused EUV light is difficult. A good vacuum is needed for starters and focusing must be done by lossy reflectors rather than lenses. Then there is the higher energy of the EUV photon, which can result in diffuse damage to the photoresist and obliterate the precision achieved with the fine optical resolution.

(U) Until recently, EUV photoresist sensitivity was referenced to a measurement technique developed at Sandia National Laboratories[9] in the late 1990s. Then scientists[10] at the Advanced Light Source at Lawrence Berkeley National Laboratory used a National Institute of Standards and Technology (NIST)-calibrated photodetector to check the standard. The results showed the baseline resists were approximately 1.9 times faster than previously thought, which implies that half as much light energy as had been expected is arriving at the wafer.

(U) All this requires a significant departure from deep UV lithography, i.e., new, even more expensive fabs and what would be the biggest change in lithography in 50 years. Commercial EUV production systems capable of 28-nm half-pitch patterns should appear in 2010, but they will be too slow for industrial scale production. Lens designers at Carl Zeiss[6] believe they can build optics capable of reaching at least an 11-nm half-pitch, but, as mentioned, the optics may not be the limiting factor.

Given the diverging requirements for memory and logic, *e.g.*, memory doesn't require as many masks and is more regular, it is entirely possible that different solutions will emerge for each. This could drive up the cost of development of new technologies that would need to be built on a smaller base.

2.3.3 (U) X-ray Beams

(U) Beyond EUV in the energy spectrum are X-rays and gamma rays. The challenges presented by X-ray lithography may make EUV seem like a walk in the park. For starters, there is the challenge of building a source that is both luminous and compact (synchrotrons hundreds of meters—or kilometers—in diameter are impractical), but progress is being made.[11] Another challenge is the optics. X-rays of course pass through most objects and are reflected very efficiently only at very shallow angles—akin to skipping stones on water. Again, progress is being made. An MIT group[12] has fabricated a new, highly

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[9] (U) Brainard, R.L., C. Henderson, J. Cobb, "Comparison of the lithographic properties of positive resists upon exposure to deep- and extreme-ultraviolet radiation," *J. Vac. Sci. Technol. B*, **17**(6), 3384-3389 (November 1999) [doi:10.1116/1.591015]

[10] (U) Naulleau, P.P., E.M. Gullikson, A. Aquila, S. George, and D. Niakoula, "Absolute sensitivity calibration of extreme ultraviolet photoresists," *Optics Express*, **16**(15), 11519-11524 (21 July 2008) [online]

[11] (U) Nakajima, K., "Compact X-ray sources: Towards a table-top free-electron laser," *Nature Physics*, **4**, 92-93 (2008) [doi:10.1038/nphys846]

[12] (U) Heilmann, R.K., M. Ahn, E.M. Gullikson, and M.L. Schattenburg, "Blazed high-efficiency X-ray diffraction via transmission through arrays of nanometer-scale mirrors," *Optics Express*, **16**(12), 8658-8669 (9 June 2008) [online]

efficient nanoscale Venetian-blind-like device that contains thousands of ultrasmooth mirror slats per millimeter. The silicon slats—as thin as 35 nm—are parallel to each other and separated by as little as about 150 nm. The slats extend many micrometers in the other two dimensions. The so-called Critical-Angle Transmission (CAT) gratings feature dense arrays of tens-of-nanometer-thin, freely suspended silicon structures that serve as efficient mirrors for the reflection and diffraction of nanometer-wavelength light. The concept behind this design may also be applicable to EUV and even neutron optics and for diffracting electrons, atoms, and molecules

2.3.4 (U) Electron Beams

(U) With electron beam lithography, a beam of electrons is scanned across a resist covered surface to create an image much the way older cathode-ray tube televisions worked, although newer systems now use vector scanning rather than raster scanning. In either case the scan time is a major impediment to high-volume manufacturing. On the positive side, since electrons have much shorter wavelengths than photons the resolution is potentially quite high, with beam widths routinely going down to a few nanometers. As with EUV, the energy of the electrons can be a problem, resulting in proximity effects where the developed pattern in wider than the scanned pattern due to scattering of both primary and secondary (from impact ionization) electrons. Low-energy electrons, such as with a scanning tunneling microscope, can be used, but this makes high resolution more difficult. High-energy electrons, as with transmission electron microscopes, can be used to sputter the resist, but this is very inefficient and requires even longer exposure times. This technology seems well suited to building individual nanoscale devices in a laboratory, but shows no sign of scaling to production level use.

2.3.5 (U) Imprints

(U) Imprint lithography, or more specifically nanoimprint lithography, creates patterns by mechanical deformation of the resist. It is a simple pattern transfer process that is not limited by wavelength and does not have to deal with secondary electrons, but it does have problems with defects and the pressure needed to create the imprint. It is a relatively new (1996) technology [13] that has yet to break out of the laboratory, although Chou, who developed the technique, continues to make progress and is now working in the sub-10-nm [14] regime. He has also used the technique to cut and exfoliate graphene [15] islands and transfer print them into device active-areas on a substrate with a placement accuracy potentially in nanometers. Working FETs with good transport properties were achieved (hole and electron mobility of 3735 and 795 cm^2/V-s, respectively, and a maximum drive-current of 1.7 mA/μm (at V_{DS} = 1 V)), but the average thickness was four layers with a variation of two layers.

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[13] (U) Chou, S.Y., P.R. Krauss, P.J. Renstrom, "Imprint Lithography with 25-Nanometer Resolution," *Science*, 272(5258), 85-87 (5 April 1996) [doi:10.1126/science.272.5258.85]

[14] (U) Wang, Y., X. Liang, Y. Liang, S.Y. Chou, "Sub-10-nm Wide Trench, Line, and Hole Fabrication Using Pressed Self-Perfection," *Nano Lett.*, 8(7), 1986-1990 (10 June 2008) [doi:10.1021/nl801030c]

[15] (U) Liang, X., Z. Fu, and S.Y. Chou, "Graphene Transistors Fabricated via Transfer-Printing In Device Active-Areas on Large Wafer," *Nano Lett.*, 7(12), 3840-3844 (14 November 2007) [doi:10.1021/nl072566s]

2.3.6 (U) Self Assembly

(U) Self-assembled structures using block copolymers (BCPs), two chemically dissimilar polymers joined together, are emerging as a promising route to generate templates and scaffolds for the fabrication of nanostructured materials. Macro-scale ordered arrays of cylindrical microdomains 3 nm in diameter (6.9 nm center to center), with areal densities in excess of 10 terabits per square inch, have been produced.[16] Working, addressable bits have not been demonstrated, but the process looks promising.

2.3.7 (U) Metamaterials and Superlenses

(U) Almost in the realm of science fiction is the use of metamaterials, which are artificially designed subwavelength composites possessing extraordinary optical properties that do not exist in nature. They can alter the propagation of electromagnetic waves, resulting in negative refraction, subwavelength imaging, and cloaking. While it is cloaking that has caught the imagination of the public and the press, it is subwavelength imaging with a superlens that could revolutionize the semiconductor lithographic process and provide a commercial path to nanoscale devices. The theoretical basis for a superlens was described by John Pendry[17] in 2000. Pendry observes that "Our simulations show that a version of the lens operating at the frequency of visible light can be realized in the form of a thin slab of silver. This optical version resolves objects only a few nanometers across." Realizing a real superlens has proved challenging but steady progress is being made. In 2008 Zhang[18] and his group at the Berkeley Molecular Foundry formed a metamaterial from silver nanowires which were electrochemically deposited in porous aluminum oxide. The resulting material exhibits negative refraction down to 660 nm, so it is the first bulk metamaterial to possess a negative index in the visible region of optics. Technically, to achieve a negative index of refraction in a metamaterial, its values for permittivity - the ability to transmit an electric field - and permeability - how it responds to a magnetic field - must both be negative. The experiment did not quite accomplish this because only the transverse magnetic-polarized light undergoes a negative refraction; the transverse electric-polarized light undergoes a positive refraction. Negative n (-0.6) at 780 nm has also been obtained[19] with low losses using a fishnet arrangement and -1.23 at 1775 nm,[20] with the material showing a negative index over a broad spectral range in the infrared sufficient to construct a prism.

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[16] (U) Park, S., D.H. Lee, J. Xu, B. Kim, S.W. Hong, U. Jeong, T. Xu, and T.P. Russell, "Macroscopic 10-Terabit–per–Square-Inch Arrays from Block Copolymers with Lateral Order," *Science*, **323**(5917), 1030-1033 20 February 2009) [doi:10.1126/science.1168108]

[17] (U) Pendry, J., "Negative Refraction Makes a Perfect Lens," *Phys. Rev. Lett.*, **85**(18), 3966-3969 (30 October 2000) [doi:10.1103/PhysRevLett.85.3966]

[18] (U) Yao, J., Z. Liu, Y. Liu, Y. Wang, C. Sun, G. Bartal, A.M. Stacy, and X. Zhang, "Optical Negative Refraction in Bulk Metamaterials of Nanowires," *Science*, **321**, 930 (15 August 2008) [doi:10.1126/science.1157566]

[19] (U) Soukoulis, C.M., S. Linden, and M. Wegener, "Negative Refractive Index at Optical Wavelength," *Science*, **315**, 47-49 (5 January 2007) [doi:10.1126/science.1136481]

[20] (U) Valentine, J., S. Zhang, T. Zentgraf, E. Ulin-Avila, D.A. Genov, G. Bartal, and X. Zhang, "Three-dimensional optical metamaterial with a negative refractive index," *Nature*, **455**, 376-379 (11 August 2008) [doi:10.1038/nature07247]

(U) There is a need for alternative, improved and simplified designs that can be easily fabricated and experimentally characterized, especially in the infrared and optical regions of the spectrum. A short-wire-pair can behave like a split ring resonator, exhibiting a magnetic resonance followed by a negative permeability regime. Moreover, short-wire-pairs can give simultaneously a negative ε in the same frequency range, and therefore a negative n, without the need for additional continuous wires. Experiments had not shown evidence of negative n at THz frequencies in the short wires-pair cases that were studied, but new designs of short-wire-pair based metallic structures show negative index of refraction in the different regimes.[21]

2.3.8 (U) Nonlinear Optics

(U) Imaging directly through a nonlinear medium is currently not possible because intensity-dependent phase changes distort the image as the wave propagates through the material. The reconstruction of nonlinear pulses in fibres has been demonstrated using the techniques of digital holography. Two steps are required: recording the total field (both amplitude and phase) exiting a nonlinear medium and numerically back-propagatin g the wavefunction. Recently a Princeton group[22] has extended this process to two-dimensional spatial beams and demonstrated a self-defocusing photorefractive crystal, showing examples in soliton formation, dispersive radiation, and imaging. For known nonlinearity, the technique enables reconstruc tion of wave dynamics within the medium and suggests new methods of super-resolved imaging, including subwavelength microscopy and lithography. The Princeton system (see Figure 2.3) has as its core component a nonlinear wave mixer, a rectangular pill-sized crystal of strontium barium niobate. An AirForce chart widely used to calibrate optical devices was used to demonstrate the high resolution of the system. As shown on the left of the figure, a normal lens doesn't capture all the rays resulting in a blurry image. The nonlinear material on the right combines the original rays to create new ones (in red), resulting in an image that is scrambled but one that can be unscrambled with a computer to yield a crisp wide-field image. For lithography, the mask image would need to be first scrambled by the computer before being projected onto the chip.

[21] (U) Dolling, G., M. Wegener, C.M. Soukoulis, and S. Linden, "Negative-index metamaterial at 780 nm wavelength," *Opt. Lett.*, **32**(1), 53-55 (1 January 2007) [doi:10.1364/OL.32.000053]
[22] (U) Barsi, C., W. Wan, and J.W. Fleischer, "Imaging throuch nonlinear media using digital holography," *Nature Photonics*, **3**, 211-215 (22 March 2009) [doi:10.1038/nphoton.2009.29]

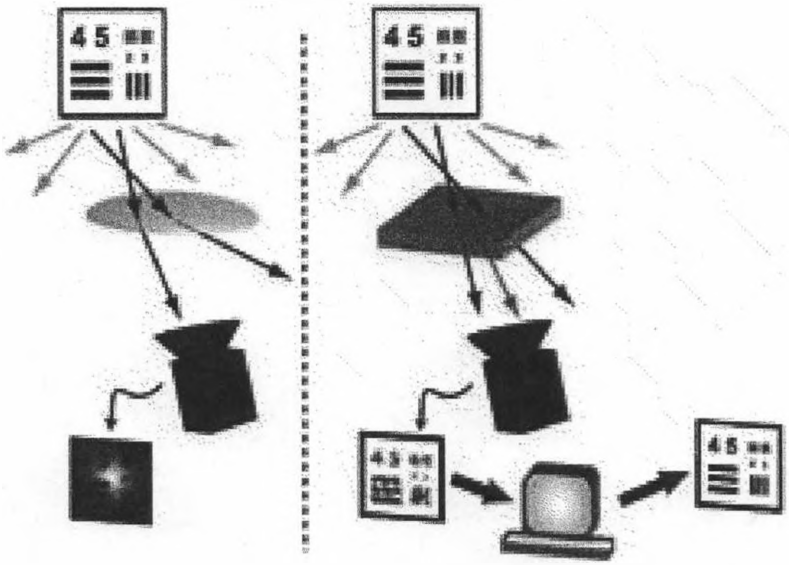

Figure 2.3. (U) Normal lens (left) and computer assisted nonlinear material system (right)[22]

2.4 (U) Other Challenges to Moore's Law

(U) In addition to the challenges presented by lithography, another problem has emerged after thirty years of scaling. Dennard assumed that the threshold voltage (V_T) would scale along with the operating voltage, providing both improved performance and power efficiency. Sub-threshold leakage was relatively low in the seventies and was negligible on logic circuits, but now leakage is making it very difficult to scale operating voltage and hence performance. A growing fraction of the power put into a transistor goes to heating the chip and not making it switch faster. This is the result of the end of gate oxide thickness scaling. Intel's 65 nm generation transistors use a silicon dioxide dielectric only five atoms thick (1.2nm). Dennard assumed that channel doping could be kept appropriate for shorter channel lengths, but when channel doping gets too high the carrier mobility and performance degrade due to increased scattering from the impurities and leakage increases due to tunneling. Higher dielectric materials such as hafnium oxide are being used to help minimize the leakage, but the fundamental problem remains.

(U) Less well known is Dennard's scaling rules for interconnects. Unlike transistors, scaled interconnects do not speed up. The reduction in line capacitance is offset by an increase in resistance. This was not much of an issue in 1974, when interconnect delay was a small fraction of the clock cycle time, but this is no longer the case. Current strategies include adding more metal layers, converting from aluminum to more conductive copper wires, and replacing SiO_2 dielectrics with low-κ dialectics, such as HfO, to reduce capacitance.

(U) The nineties saw exceptional improvements in processor clock speeds, going from the 40 MHz Motorola 68040 in 1990 to the 2 GHz Pentium 4 in 2000; a factor of fifty in just ten years, a doubling period of every 21 months and better than the Moore's Law doubling rate of every 24 months. Some of this accelerated improvement was due to exploitations of Dennard scaling as explained above. Over the entire period of integrated circuits, however, the doubling rate for clock speeds has been closer to three

years as shown in Figure 2.4. If the trend were to continue we could expect 100 GHz processors in 2020 and 1.1 THz in 2030. Unfortunately the doubling rate has dropped significantly more recently as the impacts of the end of Dennard scaling have become apparent. It took four years and two technology generations for the clock speed to almost double from 2.4 GHz in 2003 to 4.7 GHz in 2007.

(U) Although in a narrow sense Moore's Law is about the number of components (transistors) on a chip, many measures of computational performance have been strongly linked to it, including processing speed, memory and storage capacity, and communication speed.

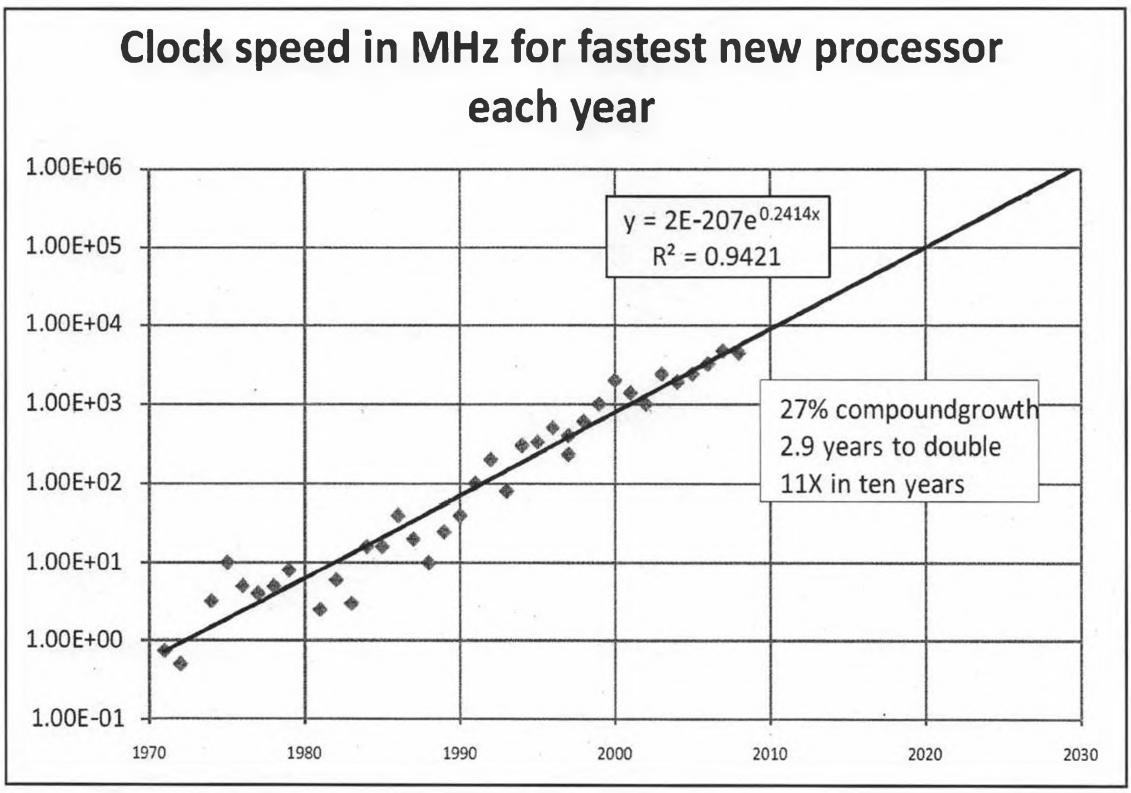

Figure 2.4. (U) Exponential growth of processor clock speed

2.5 (U) Roadmap

(U) The International Technology Roadmap for Semiconductors (ITRS), which produces a full report in odd-numbered years (2007[23]) and updates the report in even-numbered years (2008[24]), is one of the principal guidelines for technology assessment concerning whether or not Moore's Law is likely to be sustained in the future. The ITRS attempts to distinguish the different maturity or confidence levels of the principal technology "targets" needed to sustain Moore's Law, with four categories ranging from

[23] (U) *International Technology Roadmap for Semiconductors: 2007 Edition*, L. Wilson, ed., 2007; http://www.itrs.net/Links/2007ITRS/Home2007.htm.
[24] (U) *International Technology Roadmap for Semiconductors: 2008 Update*, 2008 http://www.itrs.net/Links/2008ITRS/Home2008.htm.

"solutions exist and are being optimized" to "manufacturable solutions are NOT known." The latter are highlighted in red in the tables indicating where progress might end if tangible breakthroughs are not achieved. Although some areas show red as soon as 2010, *e.g.*, oxide thickness and leakage current for high-performance logic devices, others, such as DRAM and non-volatile memory, have sections that don't go red until 2021 (or not for the foreseeable future).

(U) The roadmap rightly points out that, while silicon-based CMOS (Complementary Metal-Oxide-Silicon) technologies benefit from the "downscaling of minimum dimensions [that] enables the integration of an increasing number of transistors on a single chip, as described by Moore's Law," other requirements, *e.g.*, power consumption and communications bandwidth, do not. The use of non-CMOS solutions, which may eventually be integrated with CMOS, requires innovations in cross-disciplinary fields, such as nano-electronics, nano-thermomechanics, nano-biology, etc. As atomic scale devices evolve, quantum–physical phenomena become important and the diversification the roadmap describes as "More than Moore" (heterogeneous systems, system-in-package (SIP), etc.) plays an ever greater role in expanding device capabilities. Quantum effects are proving ever more important to conventional devices and are not solely in the realm of quantum information science. For example, Nishiguchi[25] *et al.* describe a circuit that allows them to perform pattern matching by harnessing the stochastic, quantum-mechanical tunneling of single electrons into a transistor. Their device uses silicon-insulator circuits compatible with CMOS, works at room temperature, and can respond to the stimulus of a single electron.

2.5.1 (U) ITRS 2007 Report

(U) For 2007, ITRS created a new cross-disciplinary working group to produce a separate chapter on Emerging Research Materials (ERM). The scope of the new working group covers materials properties, synthetic methods, metrology, and modeling required to support future Emerging Research Devices (ERD) that were reviewed in the May 2008 issue of Computer.[26] The control of nanostructures and their properties is key to enabling high density devices, lithographic technologies, and interconnect fabrication and operation at the nanometer scale. The roadmap also makes clear that "computational material science needs to be developed and applied to contribute to the assessment and selection of these new materials in order to reduce the experimental effort, and to contribute to the databases required for semi-empirical calculations."

(U) This technology assessment and forecast will concentrate on the following areas outlined in the 2007 ERM chapter plus modeling and simulation.

- Low-Dimensional Materials
  Nanostructure materials, such as nanotubes, nanowires and nanoparticles, offering a diverse array of novel properties are the focus of this area. Of particular interest are carbon nanotubes with their uniquely high thermal conductivity, mechanical strength, current carrying ability and long ballistic

[25] (U) Nishiguchi, K., Y. Ono, A. Fujiwara, H. Inokawa, and Y. Takahashi, "Stochastic data processing circuit based on single electrons using nanoscale field-effect transistors." *Appl. Phys. Lett.* **92,** 062105 (13 February 2008) [doi:10.1063/1.2870199]

[26] (U) Bourianoff, G., J.E. Brewer, R. Cavin, J.A. Hutchby, and V. Zhirnov, "Boolean Logic and Alternative Information-Processing Devices." *IEEE Computer* **41**(5) 38-46 (May 2008) [doi: 10.1109/MC.2008.145]

transport lengths. Using nanotubes for electrical interconnect and via applications appears attractive, but growing them in controlled locations with the proper alignment remains a challenge. Graphene, the 2D analog of carbon nanotubes, shows promise for bandgap tuning through lateral size quantization, but a basic understanding (through modeling) of the factors that control graphene's properties is needed.

- Macromolecules
  Polymers, molecular glasses, dendrimers and other novel molecules enable a wide range of competitive applications of lithography, devices, ultra low-κ interlevel dielectrics and packaging. The most significant challenge is to establish models that correlate macromolecular structure with the functional performance of material matrices in complex environments. The development of molecular devices with high densities beyond CMOS is the goal.

- Directed Self Assembly
  Self assembly is a natural process driven by the thermodynamics of intermolecular repulsion on an energy landscape that can deposit aligned molecules in precise locations on surfaces or cause phase separation into locally ordered structures in block copolymers. There are two main types of self-assembly: static, which deals with equilibrium structures; and dynamic, a non-equilibrium process in which energy is supplied to the system to maintain a steady-state population of ordered structures. Two reports[27,28] show progress in combining the two types, demonstrating that novel materials may be constructed by incorporating pathway-directing information into the constituents and the process of self-assembly. Self-assembled structures have been generated with <15 nm dimensions and the ability to generate sub-10 nm structures may be possible. Not all applications require pattern registration, *e.g.*, capacitors, nanocrystals for flash memory, air gap masks, and low refractive index cladding for optical waveguides, but uniformity is a challenging requirement. Nevertheless, useful nanomaterials must be assembled in predefined locations, orientations, and morphologies, with low thermal or electrical resistance.

- Spin Materials
  Information representation using electron spin orientation, and its associated magnetic field, has lead to a variety of memory devices, but spin-based logic devices need a broader range of control, manipulation and transport mechanisms that can operate above room temperature. Unlike charge, the ability to manipulate single spins while maintaining coherency is still in its infancy. It is critical to understand the mechanisms and physical principles that determine the magnetic, electrical and optical properties of the relevant materials.

- Complex Metal Oxides
  Transition metal oxides, whether alone or in combination with group II and lanthanide metal oxides, present many bi-stable environments determined by stoichiometry that can be altered by stress, oxygen vacancies and diffusive hydrogen. These materials offer many possible novel memory or

[27] (U) Ladet, S., L. David, A. Domard, "Multi-membrane hydrogels," *Nature* **452**, 76-79 (6 March 2008) [doi:10.1038/nature06619]
[28] (U) Capito, R.M., H.S. Azevedo, Y.S. Velichko, A. Mata, S.I. Stupp, "Self-Assembly of Large and Small Molecules into Hierarchically Ordered Sacs and Membranes," *Science* **319**, 1812-1816 (28 March 2008) [doi:10.1126/science.1154586]

logic applications. Many of them have potential as spin materials and offer novel coupling of electric and magnetic properties. The recent identification of Chua's[29] missing memristor by Williams *et al.*[30] used TiO_2 complexes and could lead to ultra-dense, non-volatile memory devices.

- Interfaces and Heterointerfaces
  Interfaces between nanoscale structures and their environment dominate the performance and limit the reliability of the electronic devices as a whole; therefore it is critical to understand the correlation of interface physical and compositional nanostructure to electronic and magnetic (spin) properties.
- Modeling and Simulation
  Although not part of the ITRS ERM Chapter, material synthesis at the atomic, molecular, nano- and macro-scale requires a deep understanding of the multi-scale, multi-physics processes that are occurring. Modeling and simulation are required to provide that understanding. Significant progress has been made in extending the reach of *ab initio* methods but much needs to be done.

2.5.2 (U) ITRS 2008 Update

(U) The 2008 Emerging Research Materials (ERM) Technology Working Group (TWG) chose not to make any changes to the 2007 ERM Chapter. The group is focused on developing a critical assessment process and reviewing progress on the ERM that were identified as potential solutions to technology needs in the 2007 ITRS ERM Chapter. Based on the Joint ERD/ERM workshop on promising device technologies, the ERM will increase focus on assessment of graphene and carbon nanotubes for extreme CMOS and beyond CMOS device applications in the 2009 ERM Chapter.

(U) According to the ERM Update summary: "Low dimensional materials, such as nanotubes, nanowires, and other nanoparticles have properties that could provide solutions for Emerging Research Devices, Lithography, Front End Process, Interconnects, and Assembly and Packaging. Novel macromolecules have potential for applications in ERD, Lithography, FEP, and Assembly and Packaging. Self Assembled Materials have potential for applications in Lithography, high charge density capacitors in Assembly and Package applications, and for selective deposition or etching processes in Front End Processes. Spin materials are of primary interest for Emerging Research Device Applications. Complex metal oxides have potential for applications as Emerging Research Memory and Logic Devices. A special set of the complex metal oxides, strongly correlated electron state materials, and their heterointerfaces may have potential to enable new logic devices with coupled spin and charge properties."

(U) The lack of an update does not mean the working group was not active in 2008. "The result of the workshop held on July 12, 2008, and a following ERD/ERM working group meeting on the following day was a recommendation to the IRC [International Roadmap Committee] of 'Carbon-based Nanoelectronics' to include CNTs [carbon nanotubes], graphene, and GNRs for accelerated development and more detailed roadmapping as part of promising technologies for 5-10 years demonstration horizon.

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[29] (U) Chua, L.O., "Memristor – The missing circuit element." *IEEE Trans. Circuit Theory* **18**, 509-519 (September 1971)

[30] (U) Strukov, D.B., G.S. Snider, D.R. Stewart and R.S. Williams. "The missing memristor found." Nature **453**, 80-83 (1 May 2008) [doi:10.1038/nature06932];
http://blogs.spectrum.ieee.org/tech_talk/2008/07/memristors_coming_soon_to_a_br.html;
http://knol.google.com/k/blaise-mouttet/programmable-electronics-using/23zgkn5xnlchu/2#.

(U) The ITRS Modeling and Simulation chapter only revised the tables in the 2008 Update. This included the long-term challenge on "Nano-scale modeling for Emerging Research Devices including Emerging Research Materials" , which has been extended to also refer to interconnects, and now explicitly includes ab initio modeling tools for nanostructure materials as well as devices and carbon-based nanoelectronics. It also changed molecular electronics to atomic electronics.

2.6 (U) Low-Dimensional Materials

2.6.1 (U) Graphene

(U) Graphite, the familiar pencil-lead form of carbon, consists of layers of carbon atoms tightly bonded in the plane in the form of a hexagonal mesh but loosely bonded between planes. This allows the layers to move easily over one another and is the reason graphite is a good lubricant. The graphite layers, consisting of carbon atoms arranged in benzene-like hexagons, like a sheet of chicken wire, actually consist of graphene, which had never been observed in isolation until 2004.[31] In fact, such two-dimensional objects such as graphene (see Figure 2.5) were believed impossible to create—or even exist—as free-standing objects. The fact that free-standing graphene sheets are stable appears to be due to the observation[32] that they are not perfectly flat but exhibit intrinsic microscopic roughening such that the surface normal varies by several degrees and out-of-plane deformations reach 1 nm, giving the surface a corrugated effect that may explain, as a consequence of the broken symmetry, the suppression of weak localization that is consistent with the high mobility of charge carriers in graphene.

(U) Graphene's unusual electronic properties arise from the fact that each carbon has four valence electrons, three of which are tied up in bonding with its neighbors, leaving the fourth unbound in π-orbitals that extend above and below the plane. The quantum mechanical wavefunctions for these electrons are delocalized across the entire graphene sheet—actually above and below the sheet, the sheet itself is a node in the wavefunction with zero probability of finding the electron there. The result is that the quasiparticle charge carriers (negatively charged electrons and positively charged "holes") in graphene do not look anything like the charge carriers of ordinary semiconductors. In graphene the quasiparticles behave as massless Dirac fermions that travel at a constant speed—a small ($1/300^{th}$) but noteworthy fraction of the speed of light but four times faster than in silicon. In graphene electrons behave more like photons, i.e., they can change their momentum and energy, but they cannot speed up of slow down. Consequently, unlike electrons in other materials, the electrons in graphene can move ballistically—without collisions—over great distances (micrometers) and through impurity barriers, even at room temperature. This means graphene can conduct electrical current ten to one hundred times better than a normal semiconductor like silicon at room temperature. Since graphene is a (nearly) flat sheet it is likely to be compatible with conventional fabrication processes used by today's chipmakers.

[31] (U) Novoselov, K.S., A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, A. A. Firsov, "Electric Field Effect in Atomically Thin Carbon Films," *Science*, **306**, 666-669 (22 October 2004) [doi:10.1126/science.1102896]

[32] (U) Meyer, J.C., A.K. Geim, M.I. Katsnelson, K.S. Novoselov, T.J. Booth, and S. Roth, "The structure of suspended graphene sheets," *Nature*, **446**, 60-63 (1 March 2007) [doi:10.1038/nature05545]

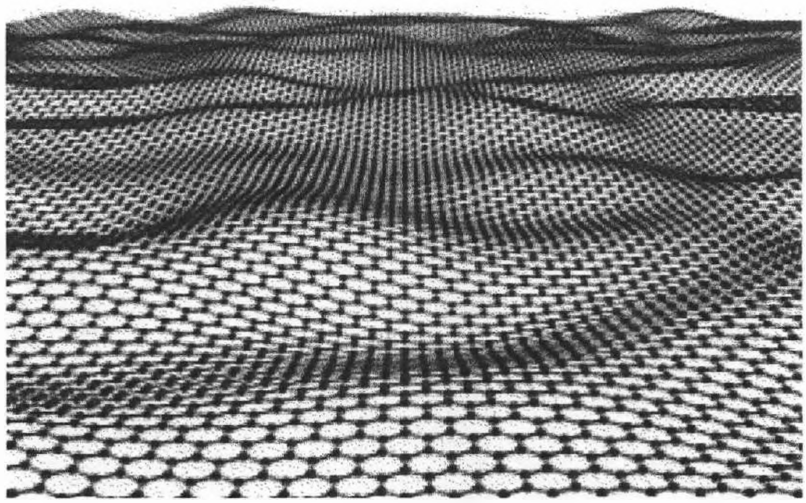

Figure 2.5. (U) A single sheet of graphene – the ripples add strength (from C&E News Cover[33])

(U) The band structure of a material determines which energy states can be occupied by its electrons, which fill lower energy states first. The electrons in the highest occupied energy level determine the Fermi level. When there are plenty of nearby energy levels that are easily reachable, the material is a metal (depicted on the left of Figure 2.6). If there is a gap between the Fermi level and the lowest unoccupied energy level, the material is a band insulator (depicted in the middle of Figure 2.6). If the gap can be controlled, say by an external field, the material is a semiconductor. The band structure of graphene (depicted on the right of Figure 2.6) is like two cones touching at the tip, with the Fermi level where the cones meet. There is no band gap so graphene is usually considered a metallic conductor, or more precisely a semimetal, but the Fermi level lies at the Dirac point where the Fermi surface is vanishingly small. This quantizes the conductivity and gives the electrons their ballistic nature, but small changes from impurities or imperfections can make big differences, resulting in regions that behave like semiconductors.

(U) Actually, the situation is even more complicated. Based on a theory that did not consider any electron-electron interactions, Wallace[34] proposed in 1947 that graphene should be a semimetal, and all the evidence to date has supported him. Nevertheless, a decade later, Linus Pauling[35] proposed that graphene should be what is today called a Mott insulator[36]. A Mott insulator does not insulate because the band is full, but because strong local electron correlations dynamically generate a charge gap by splitting a half-filled band into lower and upper Hubbard bands. Preliminary results by Drut and Lähde[37] indicate

[33] (U) Meyer, J.C., *Chemical and Engineering News*, **87**(9), cover (2 March 2009) [online]
[34] (U) P.R. Wallace, "The Band Theory of Graphite", *Phys. Rev.*, **71**(9), 622-634 (1 May 1947) [doi:10.1103/PhysRev.71.622]
[35] (U) L. Pauling, "The Nature of the Chemical Bond and the Structure of Molecules and Crystals: An Introduction to Modern Structural Chemistry", Cornell University Press, Ithica, NY, 1960.
[36] (U) P. Phillips, "Mottness", *Annals of Physics*, **321**(7), 1634-1650 (July 2006) [doi:10.1016/j.aop.2006.04.003]
[37] (U) J.E. Drut, and T.A. Lähde, "Is Graphene in Vacuum an Insulator?", *Phys. Rev. Lett.*, **102**(2), 026802(4) (16 January 2009) [doi:10.1103/PhysRevLett.102.026802]

that graphene in vacuum is likely to be an insulator. A more extended lattice Monte Carlo simulation[38] also predicts that "suspended graphene should possess an excitonic gap in the band structure." The current state of the theory is not accurate enough, however, to make a reliable prediction of the gap. If the gap is too small the result will be of mostly academic interest. Nevertheless, the advent of ultrahigh mobility suspended graphene samples may soon provide a check on Pauling's 50-year-old prediction and (perhaps) provide a better way to manufacture small, fast, reliable graphene devices.

(U) In March 2007, Andre Geim, who first reported making graphene in 2004 by repeated mechanical exfoliation of pyrolytic graphite, wrote in a review article,[39] "Graphene is a rapidly rising star on the horizon of materials science and condensed-matter physics. This strictly two-dimensional material exhibits exceptionally high crystal and electronic quality, and, despite its short history, has already revealed a cornucopia of new physics and potential applications." One of the reasons for the excitement about graphene is that quantum relativistic effects are more easily demonstrated in two-dimensional systems. Its charge carriers mimic relativistic particles that are more easily and naturally described starting with the Dirac equation rather than the non-relativistic Schrödinger equation. This makes simulations with electron-electron interactions much more challenging, but the device physics much more interesting. Ballistic electrons on the submicrometer scale at room temperature offer several tantalizing possibilities. Among them are transistors operational at teraherz frequencies and conductive sheets in which various nanometer-size structures can be carved to make single-electron-transistor (SET) circuitry. SET architecture is relatively well developed, but does not work at room temperature due to the poor stability of nanoscale materials. Graphene may change that. It may be possible that everything including conducting channels, quantum dots[40] (semiconductors whose bound charge carriers are confined in all three spatial dimensions and hence have properties between bulk semiconductors and discrete molecules), barriers and interconnects can be cut out from a graphene sheet. Geim wrote in his 2007 review, however, that "'graphenium' microprocessors are unlikely to appear for the next 20 years." Note that a teraherz processor based on graphene in 2027 is slightly ahead of the exponential growth in clock speeds shown in Figure 2.4.

[38] (U) J.E. Drut and T.A. Lähde, "Lattice field theory simulations of graphene", *Phys. Rev. B*, **79**(16), 165425(14) (20 April 2009) [doi:10.1103/PhysRevB.79.165425]
[39] (U) Geim, A.K. and K.S. Novoselov, "The rise of graphene," *Nature Materials*, **6**(3), 183-191 (March 2007) [doi:10.1038/nmat1849]
[40] (U) Ponomarenko, L.A., F. Schedin, M. I. Katsnelson, R. Yang, E. W. Hill, K. S. Novoselov, A. K. Geim, "Chaotic Dirac Billiard in Graphene Quantum Dots," *Science*, **320**, 356-358 (18 April 2008) [doi:10.1126/science.1154663]

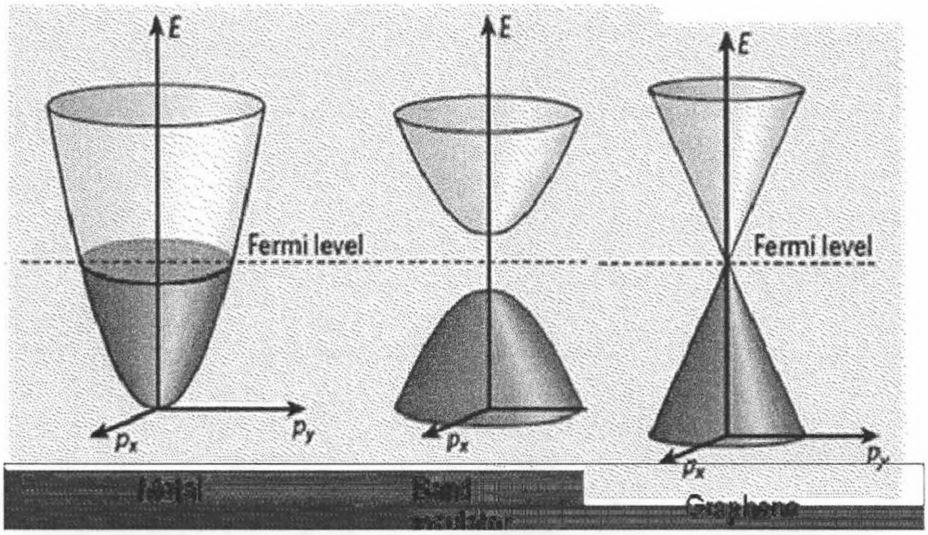

Figure 2.6. (U) The electronic energy states of a metal, a band insulator (semiconductor) and graphene[53]

(U) Characterizing the properties of graphene has been an object of intense research. The theoretical requirement that the Fermi energy—the highest occupied quantum state—be proportional to the square root of the carrier density (unlike conventional semiconductors where the relationship is linear) has been verified by a group in Berkeley,[41] but other intriguing surprises have emerged. The Berkeley group observed that "many-body interactions" seemed more complex than predicted by a simple "single-particle" model of graphene. This was indicated by the higher than expected absorbance of light at low energy—below twice the Fermi energy. They also observed that the speed of electrons in graphene *increased* as their energy was lowered, a possible result of electron-electron interactions predicted by theory—or an artifact of samples studied.

(U) Over ten years ago a Japanese group predicted,[42] using tight binding band calculations on what would now be called graphene nanoribbons (2-20 nm in width) or GNRs, that ribbons with a so-called zigzag edges would be metallic while those whose "chicken-wire" was rotated ninety degrees to the armchair orientation would be semiconductors (see Figure 2.7). Other calculations[43] have suggested that nanoribbons can conduct spin currents as well and could possibly serve as the basis for nanoscale spintronic devices.[44]

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[41] (U) Li, Z.Q., E. A. Henriksen, Z. Jiang, Z. Hao, M. C. Martin, P. Kim, H. L. Stormer and D. N. Basov, "Dirac charge dynamics in graphene by infrared spectroscopy," *Nature Physics*, **4**(7), 532-535 (July 2008) [doi:10.1038/nphys989]

[42] (U) Fujita, M., K. Wakabayashi, K. Nakada and K. Kusakabe, "Peculiar Localized State at Zigzag Graphite Edge," *J. Phys. Soc. Jpn.*, **65**(7), 1920-1923 (July 1996) [doi:10.1143/JPSJ.65.1920]

[43] (U) Yang, L., C.-H. Park, Y.-W. Son, M. L. Cohen, S. G. Louie, "Quasiparticle Energies and Band Gaps in Graphene Nanoribbons," *Phys. Rev. Lett.*, **99**(18), 186801(4) (2 November 2007) [doi:10.1103/PhysRevLett.99.186801]

[44] (U) Kusakabe, K., "Possible nano-spintronics devices with graphene as electron wave guides," *2009 APS March Meeting*, March 16-20, 2009, Pittsburgh [abstract online]

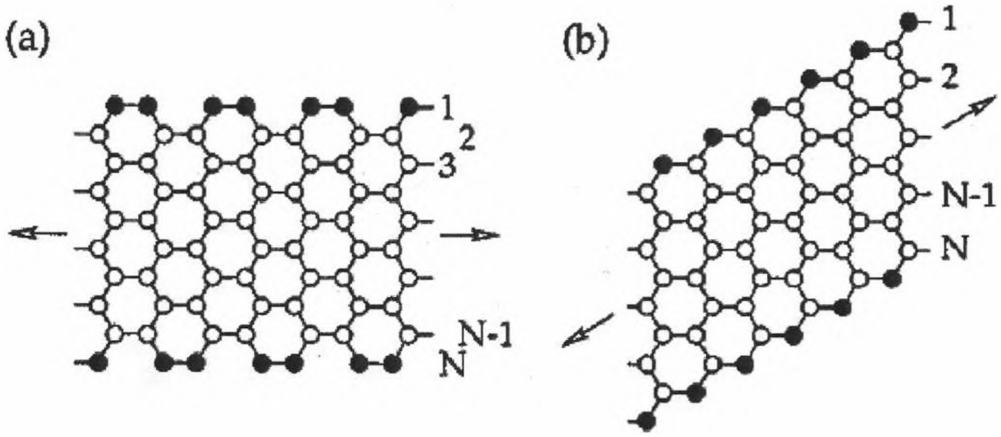

Figure 2.7. (U) "Chicken wire" nanoribbon: (a) armchair ribbon, (b) zigzag ribbon[45]

(U) Theoreticians [46] have also recently proposed yet another interesting form of graphene, "nanoroads" of pristine graphene carved in the electrically insulating matrix of graphane sheets. Two nanoroads are shown in Figure 2.8.

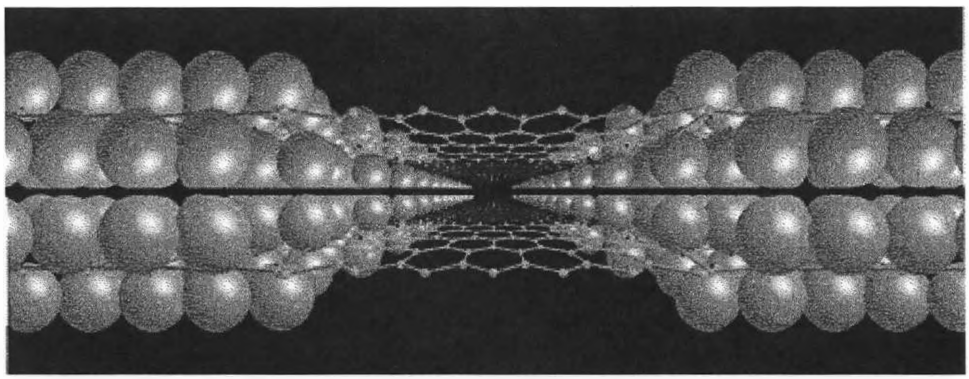

Figure 2.8. (U) Two graphane sheets with graphene nanoroads between them

(U) There had been no experimental confirmation of the nanoribbon edge effect—it loses its impact on larger graphene structure. In fact, some have observed all sub-10-nm GNRs produced have been semiconductors. [47] However, Joseph Lyding at the University of Illinois Urbana-Champaign and his student Kyle Ritter (now at Micron) used a scanning tunneling microscope to probe the electronic

[45] (U) Nakada, K., M. Fujita, G. Dresselhaus, and M.S. Dresselhaus, "Edge state in graphene ribbons: Nanometer size effect and edge shape dependence," *Phys. Rev. B*, **54**(24), 17954-17961 (15 December 1996) [doi:10.1103/PhysRevB.54.17954]

[46] (U) Singh, A.K. and B.I. Yakobson, "Electronics and Magnetism of Patterned Graphene Nanoroads," *Nano Lett.*, **9**(4), 1540-1543 (18 March 2009) [doi:10.1021/nl803622c]

[47] (U) Li, X., X. Wang, L. Zhang, S. Lee, and H. Dai, "Chemically Derived, Ultrasmooth Graphene Nanoribbon Semiconductors," *Science*, **319**, 1229-1232, (29 February 2008) [doi:10.1126/science.1150878]

structure of the graphene with atomic-scale resolution[48] and verified the prediction. The paper concludes "controlled engineering of the graphene edge structure will probably be required for obtaining uniform performance among graphene-based nanoelectronic devices."

(U) Another Berkeley Lab group,[49] using a transmission electron aberration-corrected microscope with 0.05 nm resolution, has produced visual verification of the formation and (preferred) stability of zigzag edges as can be seen in Figure 2.9. In this case mechanically exfoliated graphene was suspended in an observation grid and an electron beam was use to burn a hole into the hexagonal lattice. The zigzag pattern is clearly visible on the left and right sides of the hole while an armchair edge can be seen at the bottom.

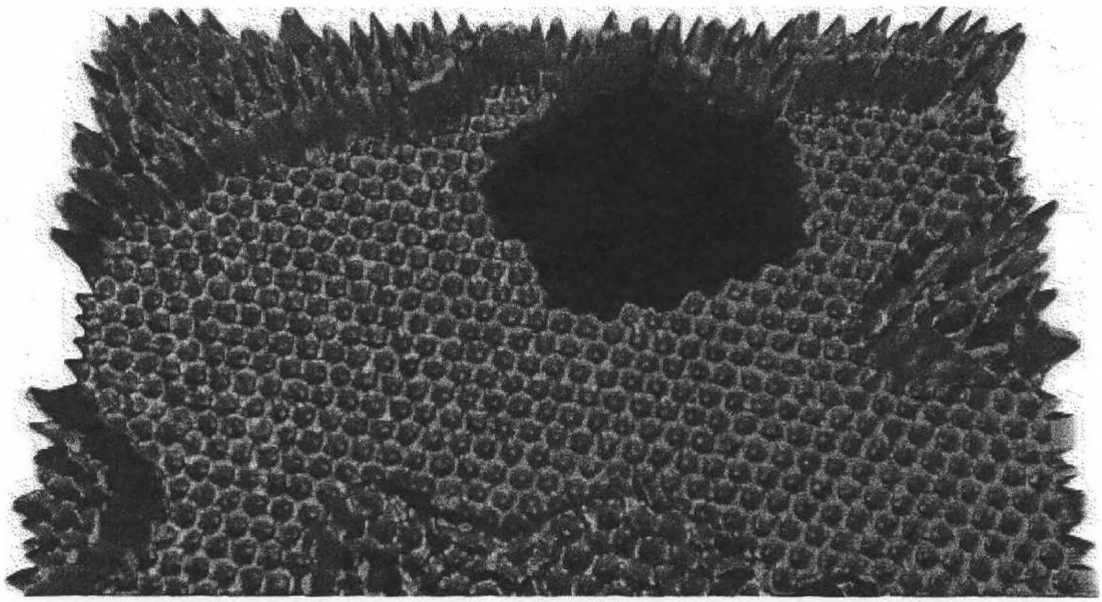

Figure 2.9. (U) A three-dimensional rendering of a graphene hole imaged on TEAM 0.5 showing the carbon atoms along the edge assume either a zigzag (more stable) or armchair configuration (courtesy of DOE/Lawrence Berkeley National Laboratory)

[48] (U) Ritter, R.A. and J.W. Lyding, "The influence of edge structure on the electronic properties of graphene quantum dots and nanoribbons," *Nature Materials* Published online: 15 February 2009 [doi:10.1038/nmat2378]
[49] (U) Girit, Ç.Ö., J.C. Meyer, R. Erni, M.D. Rossell, C. Kisielowski, L.Yang, C.-H. Park, M.F. Crommie, M.L. Cohen, S.G. Louie, and A. Zettl, "Graphene at the Edge: Stability and Dynamics," *Science*, **323**(5922), 1705-1708 (27 March 2009) [doi:10.1126/science.1166999]

(U) Graphene may also be converted from a highly conductive zero-overlap semimetal into a band insulator by exposing it to atomic hydrogen.[50] This disrupts the aromaticity of the carbon, switching the sp^2 bonds to sp^3 bonds so the carbons buckle and forms graphane, with two planes of carbon rather than one. Graphane is a semiconductor. The reaction is reversible so that the original metallic state, the lattice spacing and even the quantum Hall effect can be restored by annealing. The experiment used micromechanically cleaved graphite placed on top of a 300 nm thick layer of SiO_2. A similar experiment[51] showed that single-layer graphene is more easily hydrogenated than two-layer graphene, which is attributed to the lack of π-stacking. Also, dehydrogenated graphene on SiO2 is activated and exhibits enhanced chemical doping caused by oxygen molecules when photothermally heated. The bound oxygen molecules lead to reversible hole doping of graphene.

(U) Another approach to controlling the electronic properties of graphene is based on theoretical results[52] that show that the band structure of graphene deposited on a SiO_2 surface strongly depends on the characteristics of the surface. For an oxygen-terminated surface, the graphene monolayer exhibits a finite energy band gap while the band gap is closed when the oxygen atoms on the substrate are passivated with hydrogen atoms. Apparently the oxygen lone-pair interacts weakly with the graphene π-orbitals and results in a van der Waals attraction much weaker than covalent or hydrogen bonding. The presence of hydrogen blocks this interaction and the resulting band structure is that of isolated (metallic) graphene. This suggests that graphene could be the ideal material in which to study transitions of metals to insulators.[53] It also suggests mechanisms for tuning the electronic properties of graphene.

(U) Using SiC instead of SiO_2, Guisinger *et al.*[54] epitaxially grew single layer graphene and exposed it to atomic hydrogen in an effort to passivate the surface and interface states and alter the electronic properties of the graphene in a controlled way. Passivation of the graphene-free regions of the substrate was successful, but hydrogen did not diffuse through the graphene monolayer, suggesting that the edge of the graphene is chemically bound to the reconstructed SiC surface. Hydrogen adsorption on the graphene (yielding graphane?) results in a dramatic change in the local density of states over a spatial region much larger than the atomic adsorption sites.

(U) A recent news article in *Science*[55] reports, "The hottest material in physics these days is graphene, sheets of carbon just a single atom thick. Graphene is flexible yet harder than diamond. It conducts electricity faster at room temperature than anything else. And it's nearly transparent, a handy property for devices such as solar cells and displays that need to let light through. The only trouble is that people have

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[50] (U) Elias, D.C., R. R. Nair, T. M. G. Mohiuddin, S. V. Morozov, P. Blake, M. P. Halsall, A. C. Ferrari, D. W. Boukhvalov, M. I. Katsnelson, A. K. Geim, K. S. Novoselov, "Control of Graphene's Properties by Reversible Hydrogenation: Evidence for Graphane," *Science*, **323**, 610-613 (30 January 2009) [doi:10.1126/science.1167130]

[51] (U) Ryu, S., M.Y. Han, J. Maultzsch, T.F. Heinz, P. Kim, M.L. Steigerwald and L.E. Brus, "Reversible Basal Plane Hydrogenation of Graphene," *Nano Lett.*, **8**(12), 4597-4602 (18 November 2008) [doi:10.1021/nl802940s]

[52] (U) Shemella, P. and S.K. Nayak, "Electronic structure and band-gap modulation of graphene via substrate surface chemistry," *Appl. Phys. Lett.*, **94**(3), 032101(3) (19 January 2009) [doi:10.1063/1.3070238]

[53] (U) Fuhrer, M.S. and S. Adam, "Carbon Conductor Corrupted," *Nature*, **458**(7234), 38-39 (5 March 2009) [doi:10.1038/458038a]

[54] (U) Guisinger, N.P., G.M. Rutter, J.N. Crain, P.N. First and J.A. Stroscio, "Exposure of Epitaxial Graphene on SiC(0001) to Atomic Hydrogen," *Nano Lett.*, **9**(4) 1462-1466 (20 March 2009) [doi:10.1021/nl803331q]

[55] (U) Robert F. Service, News Focus, *Science* **322**, 1785 (19 December 2008) [doi: 10.1126/science.322.5909.1785]

been able to make only small flakes of the stuff--*until now* [emphasis added]." Jing Kong *et al.*[56] at MIT have described a low cost and scalable technique using chemical vapor deposition (CVD) to grow high-quality graphene films and then transfer them wherever they want. When graphene was first reported in 2004, single layers were peeled off chunks of graphite with clear tape—a low-tech approach hardly suitable for industrial use. Shortly thereafter graphene films were grown on silicon carbide substrates. Silicon carbide is expensive and requires an expensive ultra-high vacuum. Kong's group deposited nickel on a standard silicon wafer using conventional CVD. By patterning the nickel layer she was able to place the graphene wherever it was needed. Furthermore, her group was able to transfer the graphene films to a nonspecific substrate. This was accomplished using a support material (poly[methyl methacrylate], PMMA), wet-etching the underlying nickel film, transferring the PMMA/graphene membrane and dissolving the PMMA with acetone. The graphene film could be strongly attached to almost any material, including semiconductors, glass, metals and plastics, via van der Waals interactions.

(U) This approach (CVD on Ni) was postulated by Geim (who also considered platinum) in his review article. Its validity was quickly and independently demonstrated by Hong *et al.*[57] in Korea at Sungkyunkwan University in collaboration with Samsung and outlined in Figure 2.10. They conclude that "patterned films can easily be transferred to stretchable substrates by simple contact methods, and the number of graphene layers can be controlled by varying the thickness of the catalytic metals, the growth time and/or the ultraviolet treatment time. Because the dimensions of the graphene films are limited simply by the size of the CVD growth chamber, scaling up can be readily achieved, and the outstanding optical, electrical and mechanical properties of the graphene films enable numerous applications including use in large-scale flexible, stretchable, foldable transparent electronics."

(U) Meanwhile progress is being made in constructing graphene-based field effect transistors. Avouris *et al.*[55] at IBM report the fabrication of a top-gated graphene transistor (shown in Figure 2.11) operating at a frequency of 20GHz with a gate length of 150nm. Although this is an order of magnitude slower than the fastest silicon transistor (a single silicon-germanium transistor has operated at over 500 GHz at liquid helium temperatures and 350 GHz at room temperature[59]), they indicate that these results are consistent with a THz graphene FET with a gate length of 50 nm (well above the size where the edge effects discussed above occur) and a carrier mobility of 2000 $cm^2/V \cdot s$. This is two orders of magnitude less than the best[60,61,62] reported values of over 200,000 $cm^2/V \cdot s$, indicating significant room for

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[56] (U) Reina, A., X. Jia, J. Ho, D. Nezich, H. Son, V. Bulovic, M. S. Dresselhaus, and J. Kong, "Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition." *Nano Lett.*, **9**(1), 30-35 (January 2009) [doi:10.1021/nl801827v]

[57] (U) Kim, K.S., Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J.-H. Ahn, P. Kim, J.-Y. Choi and B. H. Hong, "Large-scale pattern growth of graphene films for stretchable transparent electrodes." *Nature*, **457**, 706-710 (5 February 2009) [doi:10.1038/nature07719]

[58] (U) Lin, Y.-M., K.A. Jenkins, A. Valdes-Garcia, J.P. Small, D.B. Farmer, and P. Avouris, "Operation of Graphene Transistors at GHz Frequencies." *Nano Lett.*, **9**(1), 422-426 (2009) [doi:10.1021/n1803316h]

[59] (U) Georgia Tech press release: "Georgia Tech/IBM announce new chip speed record." Atlanta (20 June 2006) [online]

[60] (U) Chen, J.-H., C. Jang, S. Xiao, M. Ishigami, M.S. Fuhrer, "Intrinsic and extrinsic performance limits of graphene devices on : SiO: 2." *Nature Nanotechnology* **3**, 206-209 (01 Apr 2008), [doi: 10.1038/nnano.2008.58]

[61] (U) Bolotin, K.I., K.J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P.Kim, H.L. Stormer, "Ultrahigh electron mobility in suspended graphene." *Solid state Communications*, **146**, 351-355, (June 2008) [doi:10.1016/j.ssc.2008.02.024]

improvement. The team also found that the devices behave like conventional field-effect transistors – that is the measured current gain decreases with frequency, f, according to 1/f.

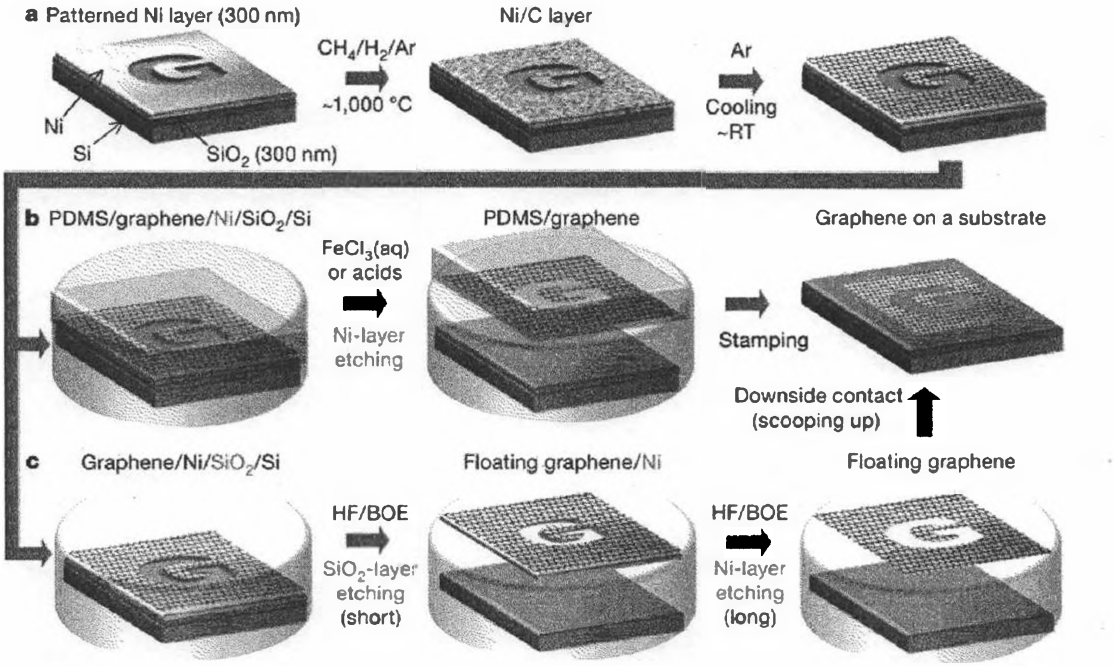

Figure 2.10. (U) Synthesis, etching and transfer process for patterned graphene films[57]

(U) The device shown in Figure 2.11 is really quite primitive and more comparable to the first transistors than the marvels of lithographic technology it aims to replace. The central piece of graphene was mechanically exfoliated and only the left side is a single layer, as shown by the TEM image in the upper right of the left frame. The left frame is the black box in the middle of the right frame, which shows the entire device.

[62] (U) Morozov, S.V., K.S. Novoselov, M.I. Katsnelson, F. Schedin, D.C. Elias, J.A. Jaszczak, and A.K. Geim, "Giant Intrinsic Carrier Mobilities in Graphene and Its Bilayer," *Phys. Rev. Lett.*, **100**(1), 016602(4) (11 January 2008) [doi: 10.1103/PhysRevLett.100.016602]

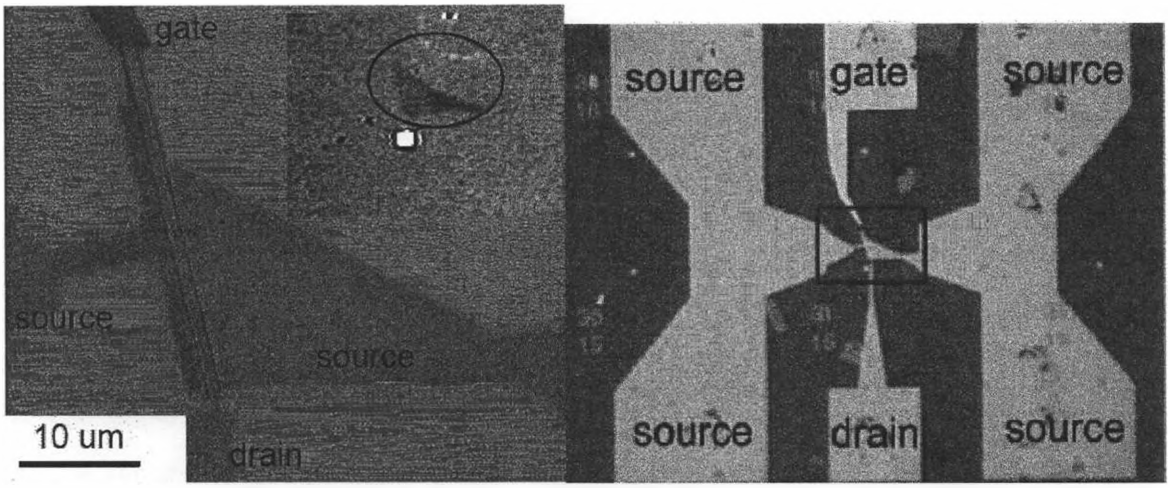

Figure 2.11. (U) Primitive 20 GHz graphene FET **Error! Bookmark not defined.**

(U) It is worth reiterating that unlike carbon nanotubes (discussed next), graphene is a flat sheet, and therefore compatible with conventional fabrication processes used by today's chipmakers. But, based on the researchers' experimental results, controlled engineering of the graphene edge structure and/or substrate will be required for obtaining uniform performance among graphene-based nanoelectronic devices. A group at MIT has recently demonstrated an efficient shaping of nanoribbon edges into zigzag or armchair edges by Joule heating.[63]

(U) The mass production of nanoribbons has also received considerable attention. Approaches include chemical synthesis, cutting graphene sheets into ribbons, and using ultrasound to break up graphene that has had its surface modified by the non-covalent binding of polymer molecules, but these methods produce small quantities of nanoribbons. One technique for producing bulk quantities of metallic nanoribbons has been reported.[64] It involves depositing volatile carbon precursors using CVD onto a substrate where they react to form nanoribbons 20-300 nm in width with 2-40 layers thick. Kosynkin *et al.*[65] report a simple, efficient and potentially scalable technique that chemically unzips multiwalled carbon nanotubes, forming nanoribbons up to 4 micrometers long with widths of 100-500 nm and 1-30 layers thick. These larger ribbons could be used in solar panels and flexible touch displays, where cheap, transparent materials are in demand. Single-walled nanotubes were also chemically unzipped to produce narrow nanoribbons, but the initial results yielded tangled ribbons. The method seems to work well with nanotubes that have many structural defects on their surfaces (such as those made by CVD), but less well with crystalline nanotubes produced by other methods, such as laser

[63] (U) Jia, X., M. Hofmann, V. Meunier, B.G. Sumpter, J. Campos-Delgado, J.M. Romo-Herrera, H. Son, Y.-P. Hsieh, A. Reina, J. Kong, M. Terrones, and M.S. Dresselhaus, "Controlled Formation of Sharp Zigzag and Armchair Edges in Graphitic Nanoribbons." *Science*, **323**(5922), 1701-1705 (27 March 2009) [doi:10.1126/science.1166862]

[64] (U) Campos-Delgado, J., J.M. Romo-Herrera, X. Jia, D.A. Cullen, H. Muramatsu, Y.A. Kim, T. Hayashi, Z. Ren, D.J. Smith, Y. Okuno, T. Ohba, H. Kanoh, K. Kaneko, M. Endo, H. Terrones, M.S. Dresselhaus and M. Terrones, "Bulk Production of a New Form of sp^2 Carbon: Crystalline Graphene Nanoribbons," *Nano Lett.*, **8**(9), 2773-2778, (14 August 2008) [doi:10.1021/nl801316d]

[65] (U) Kosynkin, D.V., A.L. Higginbotham, A. Sinitskii, J.R. Lomeda, A. Dimiev, B.K. Price and J.M. Tour, "Longitudinal unzipping of carbon nanotubes to form graphene nanoribbons," *Nature*, **458**(7240), 872-876 (16 April 2008) [doi:10.1038/nature07872]

ablation or arc discharge. Jiao *et al.*[66] describe an alternative approach for unzipping highly crystalline multiwalled nanotubes partially embedded in a polymer film and etched by an argon plasma that produces nanoribbons 10-20 nm wide and 1-3 layers thick. These nanoribbons are semiconductors and have been used to make basic transistors.

(U) Graphene is also suggested to be an excellent candidate material for novel photovoltaic devices, including transparent electrodes[67, 68] Despite the absence of a band gap, several layers of graphene can form an interesting light harvesting layer, because of its broadband light absorption and large carrier mobilities. Several key results have been reported, regarding the other optical properties of graphene, including gate-tunable optical transitions in infrared reflectivity[69] and visible absorption spectroscopy, [70] in which the fine structure constant is directly measured, practically by the naked eye, owing to graphene's unique electronic structure. More recently, scanning photocurrent microscopy (SPCM) has been applied by Lee *et al.*,[71] to study the photoelectric properties of single layer graphene devices in conjunction with the local potential variation near metal contacts and sheet edges. Park *et al.*[72] at Cornell used scanning photocurrent microscopy to investigate the spatial mapping of photocurrent generation and collection in single layer graphene in a multielectrode geometry. They showed that a strong electric field near metal-graphene contacts leads to efficient photocurrent generation, resulting in >30% efficiency for electron-hole separation.

(U) It is also worth noting that, although much of the interest has been focused on a single graphene sheet, multiple layers may also be of interest in some contexts. According to a self consistent Hartree calculation, the band structure of ABA-stacked graphene in the presence of external gates shows an increase in the density of states in sharp contrast with bilayer graphene. [73]

2.6.2 (U) Carbon Nanotubes

(U) Carbon nanotubes can be thought of as graphene sheets that have been rolled into a single- or multi-walled cylinder, forming nanoscale 'wires' with virtually no resistance. A Nanotube is a one-dimensional material where graphene is two-dimensional, and bulk materials are three-dimensional.

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[66] (U) Jiao, L., L. Zhang, X. Wang, G. Diankov, and H. Dai, "Narrow graphene nanoribbons from carbon nanotubes," *Nature*, **458**(7240), 877–880 (16 April 2009) [doi:10.1038/nature07919]

[67] (U) Wu, J., H.A. becerril, Z. Bao, Z. Liu, Y. Chem, and P. Peumans, "Organic solar cells with solution-processed graphene transparent electrodes." *Appl. Phys. Lett.*, **92**(26), 263302(3) (1 July 2008) [doi:10.1063/1.2924771]

[68] (U) Eda, G., G. Fanchini, and M. Chhowalla, "Large-area ultrathin films of reduced graphene oxide as a transparent and flexible electronic material," *Nature Nanotechnol.*, **3**, 270-274 (6 April 2008) [doi:10.1038/nnano.2008.83]

[69] (U) Wang, F., Y. Zhang, C. Tian, C. Girit, A. Zettl, M. Crommie, and Y.R. Shen, "Gate-Variable Optical Transitions in Graphene," *Science*, **320**(5873), 206-209 (11 April 2008) [doi:10.1126/science.1152793]

[70] (U) Nair, R.R., P. Blake, A.N. Grigorenko, K.S. Novoselov, T.J. Booth, T. Stauber, N.M.R. Peres, A. K. Geim, "Fine Structure Constant Defines Visual Transparency of Graphene," *Science*, **320**(5881), 1308 (6 June 2008) [doi:10.1126/science.1156965]

[71] (U) Lee, E.J.H., K. Balasubramanian, R.T. Weitz, M. Burghard and K. Kern, "Contact and edge effects in graphene devices." *Nature Nanotechnol.*, **3**, 486-490 (29 June 2008) [doi:10.1038/nnano.2008.172]

[72] (U) Park, J., Y.H. Ahn, and C. Ruiz-Vargas, "Imaging of Photocurrent Generation and Collection in Single-Layer Graphene," *Nano Lett.*, ASAP (27 March 2009) [doi:10.1021/nl8029493]

[73] (U) Koshino, M. and E. McCann, "Gate-induced interlayer asymmetry in ABA-stacked trilayer graphene," *Phys. Rev. B*, **79**(12), 125443(5), (31 March 2009) [doi:10.1103/PhysRevB.79.125443]

Nanotubes also differ from nanoribbons in that they are doubly degenerate because of the periodic boundary condition. Quantum confinement occurs when the wavefunction of a particle has about the same dimension as the space it occupies. This occurs at the nanoscale with the consequences that the energy of the particle becomes discrete and the band gap is size dependent as a consequence. A quantum wire like a nanotube has the electron confined in two dimensions; a quantum dot has it confined in all three dimensions. With confinement the band gaps are likely to be larger than in the bulk material and more resistant to tunneling as a consequence. Tunneling can still occur, but the probability is proportional to the height of the barrier, i.e., the energy difference between gaps.

(U) All nanotubes are also expected to be very good thermal conductors along the tube, but good insulators laterally to the tube axis. The thermal conductivity of carbon nanotubes has been measured at nearly 3500 $Wm^{-1}K^{-1}$ at room temperature; [74] compare this to copper, a metal well-known for its good thermal conductivity, which only transmits 385 $Wm^{-1}K^{-1}$. Carbon nanotubes are chemically [75] and mechanically [76] stable well above room temperature. Two excellent reviews of the state-of-the-art at the end of 2007 are available [77,78] as well as an update at the end of 2008. [79]

(U) There are many different ways to roll a graphene sheet depending on how the "chicken wire" hexagonal lattice is oriented. The way the graphene sheet is wrapped is represented by a pair of indices (n,m) called the chiral vector (see Figure 2.12). The integers n and m denote the number of unit vectors along two directions in the honeycomb crystal lattice of graphene. If $m=0$, the nanotubes are called "zigzag" (the vertical edges of the lattice in Figure 2.12). If $n=m$, the nanotubes are called "armchair" (the horizontal edges of the lattice in Figure 2.12). Otherwise, they are called "chiral."

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[74] (U) Pop, E., D. Mann, Q. Wang, K. Goodson, and H. Dai, "Thermal Conductance of an Individual Single-Wall Carbon Nanotube above Room Temperature," *Nano Lett.*, 6 (1), pp 96–100 (January 2006) [doi: 10.1021/nl052145f]

[75] (U) Dresselhaus, M.S., G. Dresselhaus, P.C. Eklund, *Science of fullerenes and carbon nanotubes*; Academic Press: San Diego, 1996.

[76] (U) Saito, R., G. Dresselhaus, M.S. Dresselhaus, *Physical Properties of Carbon Nanotubes*; Imperial College Press: London, 1998.

[77] (U) Avouris, P., Z. Chen, and V.Perebeinos, "Carbon-based electronics," *Nature Nanotechnology*, **2**, 605-615 (October 2007) [doi:10.1038/nnano.2007.300]

[78] (U) Jorio, A., M.S. Dresselhaus, G. Dresselhause, eds., *Carbon Nanotubes: Advanced Topics in the Synthesis, Structure, Properties and Applications*, Springer, New York (2008) [doi:10.1007/978-3-540-72865-8]

[79] (U) Avouris, P., "Carbon nanotube electronics and photonics," *Physics Today*, **62**(1), 34-40 (January 2009) [doi:10.1063/1.3074261]

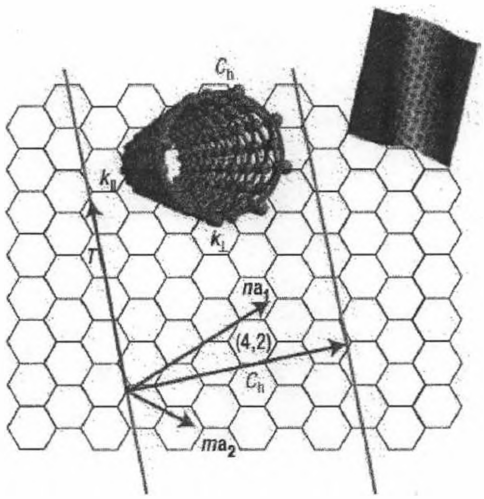

Figure 2.12. (U) The Chirality Vectors na_1 and ma_2 for a nanotube of circumference $C_h = na_1 + ma_2$ [77]

(U) Single-walled carbon nanotubes (SWCNTs, or SWNTs) have been the focus of attention for more than fifteen years since they were reported in 1993 by Ijima [80] (NEC) and Bethune *et al.* [81] (IBM), although evidence for the existence of nanotubes can be found as early as 1976. [82] SWCNTs exhibit important electric properties that are not shared by multi-walled variants. Because of the symmetry and unique electronic structure of graphene, the structure of a nanotube strongly affects its electrical properties. For a given (n,m) nanotube, if $n = m$, the nanotube is considered metallic; if $n - m$ is a multiple of 3, then the nanotube is semiconducting with a very small band gap, otherwise the nanotube is a moderate semiconductor. Thus all armchair ($n=m$) nanotubes are metallic, and nanotubes (5,0), (6,4), (9,1), etc. are semiconducting. In general, the larger the values of n and m, the larger the diameter of the nanotube, *e.g.*, (9,1) is larger, 0.75nm, than (6,4), 0.68nm. [83] In theory, metallic nanotubes can carry an electrical current density of 4×10^9 A/cm^2, which three orders of magnitude greater than metals such as copper or aluminum. [84]

(U) Despite the high current density, however, nanotubes may not be metallic in the traditional sense of having overlapping conduction and valence bands. Bockrath (Cal Tech) and Hone (Columbia) have

[80] (U) Iijima, S. and T. Ichihashi, "Single-shell carbon nanotubes of 1-nm diameter," *Nature* **363**, 603 - 605 (17 June 1993) [doi:10.1038/363603a0]
[81] (U) Bethune, D.S., C. H. Klang, M. S. de Vries, G. Gorman, R. Savoy, J. Vazquez and R. Beyers, "Cobalt-catalysed growth of carbon nanotubes with single-atomic-layer walls," *Nature* **363**, 605 - 607 (17 June 1993) [doi:10.1038/363605a0]
[82] (U) *Oberlin, A.; M. Endo, and T. Koyama, "Filamentous growth of carbon through benzene decomposition,"* Journal of Crystal Growth *32, 335–349 (March 1976) [doi:10.1016/0022-0248(76)90115-9]*
[83] (U) Wang, B., C.H.P. Poa, L. Wei, L.-J. Li, Y. Yang, and Y. Chen, "(n,m) Selectivity of Single-Walled Carbon Nanotubes by Different Carbon Precursors on Co–Mo Catalysts," *J. Am. Chem. Soc.*, **129** (29), 9014-9019 (17 February 2007) [doi:10.1021/ja070808k]
[84] (U) Hong, S. and S. Myung, "Nanotube Electronics: A flexible approach to mobility," *Nature Nanotechnology* **2**, 207 - 208 (April 2007) [doi:10.1038/nnano.2007.89]

identified Mott insulating states in nominally metallic nanotubes.[85] This indicates that "carbon nanotubes are *never* [emphasis added] metallic." They measured a gap of about ten to one hundred milli-electron volts that is inversely proportional to the radius of the nanotube. They also speculate that "the Mott gap for sub-nanometer–diameter nanotubes can be much greater than the characteristic thermal energy at room temperature and could be combined with techniques for the growth of small-diameter devices to yield room-temperature transistors."

(U) Carbon nanotubes have been widely used to study quantum dots both for basic science and research into new devices given their unique properties for studying the coherent properties of single electron spins. Steele *et al.*[86] used local gate voltages applied to an ultraclean suspended nanotube to confine a single electron in both a tunable double quantum dot. The tuning was limited by a novel type of tunneling that is "analogous to the tunneling in the Klein paradox." They observed an *increase* in current despite a *larger* barrier for tunneling. This appears to result from so-called negative energy solutions (positron states) that arise in relativistic quantum mechanics. For a barrier height that is small compared to $2mc^2$, the Dirac equation gives a wavefunction that decays exponentially inside the barrier in agreement with the non-relativistic Schrödinger equation, but for a large barrier height (comparable or greater than $2mc^2$), the negative energy solutions of the Dirac equation strongly modify the tunneling process, resulting in high probability of passing through the barrier. The increase in current is interpreted as a breakdown of the vacuum state in a high field, except the positrons are really holes. This effect could allow the development of "new types of optically active devices". A similar effect in graphene has been postulated[87], but not observed.

(U) Given the exceptional properties of SWCNTs, interest in exploiting these properties is strong and steady progress is being made and workable devices have been built, at least in the laboratory. One such device is a memory cell[88] with 100 ns write/erase speed. The endurance of these memory elements is shown to exceed 10^4 cycles. The authors believe its speed makes it competitive with state-of-the-art commercial flash memory. The authors also attribute the use of a high-κ gate dielectric (hafnium oxide) to the speed of the device, which is three orders of magnitude faster than the memory speeds of 10 ms observed earlier for devices with conventional gate oxides. The essential features of the model, and therefore the origin of the fast memory operation, are, according to the authors, "not dependent on [the] detailed structure of the SWCNT: the key issues are the defects in hafnium oxide as well as the existence and suitable location of the CNT band gap in energy and the fact that the CNT is a nanoscale, nearly ballistic conductor. Therefore, the fast memory operation demonstrated here could potentially be realized also using other carbon materials such as CNT bundles or *graphene* [emphasis added] with a band gap engineered by layer structure or reduced dimension." The fabrication of this device required direct manipulation of the SWCNTs with an atomic force microscope (AFM) using a previously reported

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[85] (U) Deshpande, V.V., B. Chandra, R. Caldwell, D.S. Novikov, J. Hone, and M. Bockrath. "Mott Insulating State in Ultraclean Carbon Nanotubes." *Science*, **323**, 106-110 (2 January 2009) [doi:10.1126/science.1165799]

[86] (U) G.A. Steele, G. Gotz, & L.P. Kouwenhoven. "tunable few-electron double quantum dots and Klein tunneling in ultraclean carbon nanotubes", *Nature Nanotechnology*, Advance online publication (6 April 2009) [doi:10.1038/nnano.2009.71]

[87] (U) A.H. Castro Neto, F. Guinea, N.M.R. Peres, K.S. Novoselov, & A.K. Geim, "The electronic properties of graphene", *Rev. Mod. Phys.*, **81**(1), 109-152 (January 2009) [doi:10.1103/RevModPhys.81.109]

[88] (U) Rinkiö, M., A. Johansson, G. S. Paraoanu, and P. Törmä, "High-Speed Memory from Carbon Nanotube Field-Effect Transistors with High-κ Gate Dielectric," *Nano Lett.* **9**(2), 643-647 (16 January 2009) [doi:10.1021/nl8029916]

technique[89] with low contact resistances between the electrodes and the carbon nanotube, down to 14 kΩ. Such "pick and place" approaches are obviously not scalable.

(U) Serious obstacles must be overcome, however, before nanotube-based devices can be used in high-volume commercial products. Among these challenges are:

- The ability to produce nanotubes with consistent size and properties
- The ability to integrate nanotubes into volume-produced devices
- The high electrical resistance at junctions between nanotubes and other metal wires.

(U) Over the past decade, significant efforts in research have been focused on finding solutions to these problems but only limited progress has been made. For example, researchers have demonstrated the separation of metallic from semiconducting SWCNTs based on electrophoresis,[90] physicochemical modification,[91,92] density gradient induced centrifugation,[93] selective elimination by electrical breakdown,[94] gas-phase plasma etching,[95] and several other methods.[96,97] However, the chemical separation methods used in these processes always introduce defects and contamination to the SWCNTs. Furthermore, the separated nanotubes still need to be assembled onto a substrate for device fabrication. Direct growth of metallic and semiconducting SWCNTs on suitable substrates would be a significant advancement and has been tried by numerous researchers.[98,99,100,101,102,103,104] Direct growth has the

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[89] (U) Zavodchikova, M.Y., A. Johansson, M. Rinkiö, J. J. Toppari [1], A. G. Nasibulin, E. I. Kauppinen, P. Törmä, "Fabrication of carbon nanotube-based field-effect transistors for studies of their memory effects," *physica status solidi (b)* **244**(11), 4188-4192 (4 October 2007) [doi: 10.1002/pssb.200776187]

[90] (U) Krupke, R., F. Hennrich, H. von Lohneysen, M.M. Kappes, "Separation of Metallic from Semiconducting Single-Walled Carbon Nanotubes" *Science*, ***301***, 344-347 (18 July 2003) [doi:10.1126/science.1086534]

[91] (U) Chattopadhyay, D, L. Galeska, F. Papadimitrakopoulos, "A Route for Bulk Separation of Semiconducting from Metallic Single-Wall Carbon Nanotubes," *J. Am. Chem. Soc.*, **125**(11), 3370 (22 February 2003) [doi:10.1021/ja028599l]

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[94] (U) Collins, P.G., M.S. Arnold, and P. Avouris, "Engineering Carbon Nanotubes and Nanotube Circuits Using Electrical Breakdown," *Science* **292** 706-709 (27 April 2001) [doi:10.1126/science.1058782]

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[96] (U) LeMieux, M.C., M. Roberts, S. Barman, Y.W. Jin, J.M. Kim, and Z. Bao, "Self-Sorted, Aligned Nanotube Networks for Thin-Film Transistors," *Science* **321** 101-104 (4 July 2008) [DOI:10.1126/science.1156588]

[97] (U) Dyke, C.A., M.P. Stewart, and J.M. Tour, "Separation of Single-Walled Carbon Nanotubes on Silica Gel. Materials Morphology and Raman Excitation Wavelength Affect Data Interpretation," *J. Am. Chem. Soc.*, **127** (12), 4497–4509 (26 February 2005) [doi: 10.1021/ja042828h]

[98] (U) Wang, B., C.H.P. Poa, L. Wei, L.-J. Li, Y. Yang, and Y. Chen, "(n,m) Selectivity of Single-Walled Carbon Nanotubes by Different Carbon Precursors on Co–Mo Catalysts," *J. Am. Chem. Soc.*, **129** (29), 9014-9019 (17 February 2007) [doi:10.1021/ja070808k]

[99] (U) Bachilo, S.M., L. Balzano, J.E. Herrera, F. Pompeo, D.E. Resasco, and R.B. Weisman, "Narrow (n,m)-Distribution of Single-Walled Carbon Nanotubes Grown Using a Solid Supported Catalyst," *J. Am. Chem. Soc.*, **125** (37), 1186–11187 (21 August 2003) [doi:10.1021/ja036622c]

potential of high purity and methods to control the alignment of growth using electric fields,[105] laminar gas flow,[106] and single crystal substrates.[107,108,109] Uniform nanotube arrays have been fabricated on a single crystal substrate,[110,111] but the coexistence of metallic and semiconducting nanotubes hinders large-scale device formation. Recently, a chemical vapor deposition (CVD) approach that allows selective growth of high density arrays of well-aligned semiconducting SWCNTs has been demonstrated.[112] Nanotubes within the arrays revealed a narrow diameter distribution from 1.55 to 1.78 nm with over 95% of nanotubes being semiconducting. The authors believe "the samples can be directly utilized for the fabrication of large amounts of FETs with standard photolithography," once the yield of semiconducting nanotubes if further refined to nearly 100%. They are also working on recipes that might yield all-metallic nanotubes.

(U) Might it be possible to directly synthesize the kind of nanotube needed for a specific application? A step in that direction was taken by a group at Berkeley's Molecular Foundry when they produced the shortest segment of a carbon nanotube, a hoop-shaped chain of benzene molecules, called

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[100] (U) Li, X., X. Tu, S. Zaric, K. Welsher, W.S. Seo, W. Zhao, and H. Dai, "Selective Synthesis Combined with Chemical Separation of Single-Walled Carbon Nanotubes for Chirality Selection," *J. Am. Chem. Soc.*, **129** (51), 15770–15771, (5 December 2007) [doi:10.1021/ja077886s]

[101] (U) Yiming Li, David Mann, Marco Rolandi, Woong Kim, Ant Ural, Steven Hung, Ali Javey, Jien Cao, Dunwei Wang, Erhan Yenilmez, Qian Wang, James F. Gibbons, Yoshio Nishi, and Hongjie Dai, "Preferential Growth of Semiconducting Single-Walled Carbon Nanotubes by a Plasma Enhanced CVD Method," *Nano Lett.*, 4(2), 317–321 (February 2004) [doi: 10.1021/nl035097c]

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[104] (U) Ciuparu, D., Y. Chen, S. Lim, G.L. Haller, and L. Pfefferle, "Uniform-Diameter Single-Walled Carbon Nanotubes Catalytically Grown in Cobalt-Incorporated MCM-41," *J. Phys. Chem. B*, **108** (2), 503–507 (16 December 2003) [doi:10.1021/jp036453i]

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[106] (U) Huang, S., B. Maynor, X. Cai, J. Liu, "Ultralong, Well-Aligned Single-Walled Carbon Nanotube Architectureson Surfaces," *Adv. Mat.*, **15**(19), 1651-1655 (7 October 2003) [doi:10.1002/adma.200305203]

[107] (U) Han, S., X. Liu, and C. Zhou, "Template-Free Directional Growth of Single-Walled Carbon Nanotubes on a- and r-Plane Sapphire," *J. Am. Chem. Soc.*, **127** (15), 5294–5295 (22 March 2005) [doi:10.1021/ja042544x]

[108] (U) Yuan, D., L. Ding, H. Chu, Y. Feng, T.P. McNicholas and J. Liu, "Horizontally Aligned Single-Walled Carbon Nanotube on Quartz from a Large Variety of Metal Catalysts," *Nano Lett.*, **8**(8) 2576–2579, (August 2008) [doi:10.1021/nl801007r]

[109] (U) Zhou, W., C. Rutherglen, P.J. Burke, "Wafer scale synthesis of dense aligned arrays of single-walled carbon nanotubes," *Nano Res.*, **1**(2), 158-165 (August 2008) [doi:10.1007/s12274-008-8012-9]

[110] (U) Kang, S.J., C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M.A. Alam, S.V. Rotkin and J.A. Rogers, "High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes," *Nat. Nanotechnol.*, **2**(4), 230 – 236 (April 2007) [doi:10.1038/nnano.2007.77]

[111] (U) Ding, L., D. Yuan and J. Liu, "Growth of High-Density Parallel Arrays of Long Single-Walled Carbon Nanotubes on Quartz Substrates," *J. Am. Chem. Soc.*, **130**(16), 5428–5429 (1 April 2008) [doi:10.1021/ja8006947]

[112] (U) Ding, L., A. Tselev, J. Wang, D. Yuan, H. Chu, T.P. McNicholas, Y. Li, and J. Liu, "Selective Growth of Well-Aligned Semiconducting Single-Walled Carbon Nanotubes," *Nano Lett.*, **9**(2), 800-805 (February 2009) [doi:10.1021/nl803496s]

cycloparaphenylene,[113] which has eluded synthesis since it was theorized more than 70 years ago. It is hoped that cycloparaphenylene molecules can be used as seeds or templates to grow large batches of carbon nanotubes with just the right specifications. Such a combination of precision and high yield will be needed if carbon nanotubes are to make the jump from the lab to the commercial sector.

(U) A different approach was taken by Kang *et al.*,[114] where they showed that: (i) amphiphilic, linear conjugated poly[p-{2,5-bis(3-propoxysulfoni cacidsodiumsalt)}phenylene]ethynylene (PPES), a linear, conformationally restricted conjugated polymer, disentangles SWNT strands from their bundled forms at high mass percent conversion; (ii) in contrast to previous studies in which other p-phenyleneethynylene-based polymers have been shown to interact with SWNTs in a parallel fashion, PPES wraps SWNTs forming a self-assembled helical super structure; and (iii) the experimentally observed PPES-SWNT helical pitch of 13 ± 2 nm is in close agreement to the 14 ± 1 nm value predicted by MD simulation. Given that conjugated polymer-SWNT blends often exhibit synergistic optoelectronic effects, this work may help guide the superhelical assembly of SWNTs with other technologically important, linear semiconducting polymers.

(U) On the other hand, some researchers have been able to exploit SWCNTs despite the disorder. Scientists[115] from Stanford University and the University of California, Los Angeles, have built a flexible supercapacitor out of printable carbon nanotubes and polymer gel electrolyte. The active electrodes were made from sprayed networks of single-walled carbon nanotubes (SWCNTs) serving as both electrodes and charge collectors. Using a printable aqueous gel electrolyte as well as an organic liquid electrolyte, the performances of the devices show very high energy and power densities (6 W h/kg for both electrolytes and 23 and 70 kW/kg for aqueous gel electrolyte and organic electrolyte, respectively) which is comparable to performance in other SWCNT-based supercapacitor devices. The results underline the potential of printable thin film supercapacitors. The simplified architecture and the sole use of printable materials may lead to a new class of entirely printable charge storage devices allowing for full integration with the emerging field of printed electronics. The first commercial printed supercapacitor could be available in five years, according to the author.

(U) Although carbon nanotubes have high thermal conductivity, nanotubes that are not chemically connected to the substrate but are bound by relatively weak van der Waals forces that have greatly reduced thermal conductance. In existing nanotube transistors only the contacts have a good thermal exchange rate, while the thermal conductance over the van der Waals separation gap is very low, of the order of 0.05-0.2 $Wm^{-1}K^{-1}$. Rotkin *et al.*[116] propose that polar substrates, such as SiO_2, or better yet, high-κ oxides, exhibit strong coupling to the surface phonon—polariton modes of the nanotube lying on the

[113] (U) Jasti, R., J. Bhattacharjee, J.B. Neaton, and C.R. Bertozzi, "Synthesis, Characterization, and Theory of [9]-, [12]-, and [18]Cycloparaphenylene: Carbon Nanohoop Structures." *J. Am. Chem. Soc.*, **130** (52), 17646–17647 (4 December 2008) [doi:10.1021/ja807126u]

[114] (U) Kang, Y.K., O.-S. Lee, P. Deria, S.H. Kim, T.-H. Park, D.A. Bonnell, J.G. Saven and M.J. Therien, "Helical Wrapping of Single-Walled Carbon Nanotubes by Water Soluble Poly(p-phenyleneethynylene)." *Nano Lett.*, **9**(4), 1414-1418 (12 March 2009) [doi:10.1021/nl803234]

[115] (U) Kaempgen, M., C.K. Chan, J. Ma, Y. Cui, and G. Grüner, "Printable Thin Film Supercapacitors Using Single-Walled Carbon Nanotubes." *Nano Lett.*, (ASAP) (6 April 2009) [doi:10.1021/nl8038579]

[116] (U) Rotkin, S.V., V. Perebeinos, A.G. Petrov, and P Avouris, "An Essential Mechanism of Heat Dissipation in Carbon Nanotube Electronics." *Nano Lett.*, ASAP, (31 March 2009) [doi:10.1021/nl803835z]

substrate and that this coupling can be used to increase the effective thermal conductance between the nanotube and the polar insulator by an order of magnitude.

(U) Carbon nanotubes have much wider uses than just electronics, which drives research even in the absence of semiconductor related devices. Other areas include composite materials, batter technology, plasma displays, sensors, hydrogen storage and desalination. Both graphene and carbon nanotubes also serve as testbeds for fundamental science, which sometimes have potential applications (spin qubits) and sometimes not (a radio built out of a single nanotube).

2.6.3 (U) Nanowires

(U) Other forms of 1-dimensional materials besides carbon nanotubes are nanowires; nanostructures with a diameter of tens of nanometers or less but unconstrained length. Nanowires can be metallic, *e.g.*, Ni, Pt, Au, semiconducting, *e.g.*, Si, InP, GaN, GaAs, etc., and insulating, *e.g.*, SiO_2,TiO_2. There are even molecular nanowires composed of repeating molecular units that can be either organic, *e.g.*, DNA, or inorganic, *e.g.*, $Mo_6S_{9-x}I_x$. As with carbon nanotubes, nanowires experience lateral quantum confinement that manifests itself as discrete values of the electrical conductance and energy levels different from the traditional continuum found in bulk materials. Nanowires, however, are much more sensitive to edge effects than carbon nanotubes. Surface defects can be a serious problem.

(U) Nanowires are being studied for use as photon ballistic waveguides as interconnects in quantum dot/quantum effect well photon logic arrays. Photons travel inside the tube, electrons travel on the outside shell. When two nanowires acting as photon waveguides cross each other the juncture acts as a quantum dot.

(U) A group at the University of Illinois Micro and Nanoelectronics Laboratory has developed a new planar growth process[117] that creates self-aligned, defect-free gallium–arsenide nanowires. It is a non-lithographic process that can precisely control the nanowires dimension and orientation, yet is compatible with existing circuit design and fabrication technology and could be readily scaled up for manufacturing purposes. The nanowires channel used in the demonstration transistor was grown by metal organic CVD using gold as a catalyst. The rest of the transistor was made with conventional techniques. The demonstration channel was a large 200 nm, but the researchers assert that nanowires with diameters of 5 nm can be made with this technique. Alignment was determined by the substrate and the nanowire was free from twin defects, rotational defects that decrease the mobility of the charge carriers. The electron mobility of the nanowire was confirmed to be as high as the corresponding bulk value.

(U) The nanowire was grown in place. In previous work Li and Fortuna[118] demonstrated they could grow the nanowires and then transfer-print them on other substrates, including silicon, for heterogeneous integration, which has applications in flexible electronics.

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[117] (U) Li, X. and S. Fortuna. *IEEE journal Electron Device Letters*, to be published.

[118] (U) Fortuna, S.A., J. Wen, I.S. Chun, and X. Li, "Planar GaAs Nanowires on GaAs (100) Substrates: Self-Aligned, Nearly Twin-Defect Free, and Transfer-Printable," *Nano Lett.*, **8**(12), 4421-4427 (10 December 2008) [doi:10.1021/nl802331m]

2.7 (U) Macromolecules

(U) Perhaps the ultimate solution to device scaling is the fabled molecular switch. If molecules could replace the current generation of transistors, you could fit more than a trillion switches onto a centimeter-square chip. In 1999, a team of researchers at Yale[119] published a description of the first such switch, but scientists have been unable to replicate their discovery or explain how it worked. As the ITRS Roadmap notes, one of the most significant challenges is to establish models that correlate macromolecular structure with the functional performance of material matrices in complex environments.

(U) Pati *et al.*[120] believe they have found the mechanism behind such a switch. For the switch in question, the current increased along with the voltage, until it rose to a miniscule 142 microamps. Then suddenly, and counterintuitively, it dropped, a phenomenon known as negative differential resistance, or NDR.A first-principles quantum transport calculation of the system (shown in Figure 2.13) was performed. Upon increasing the applied bias, it is found that a new phase in the broken symmetry wave function of the molecule emerges, a quantum phase transition, from the mixing of occupied and unoccupied molecular orbitals. As a consequence, a nonlinear change in the coupling between the molecule and the lead is evolved resulting in NDR. The model can be used to explain NDR in other classes of metal-molecule junction devices.

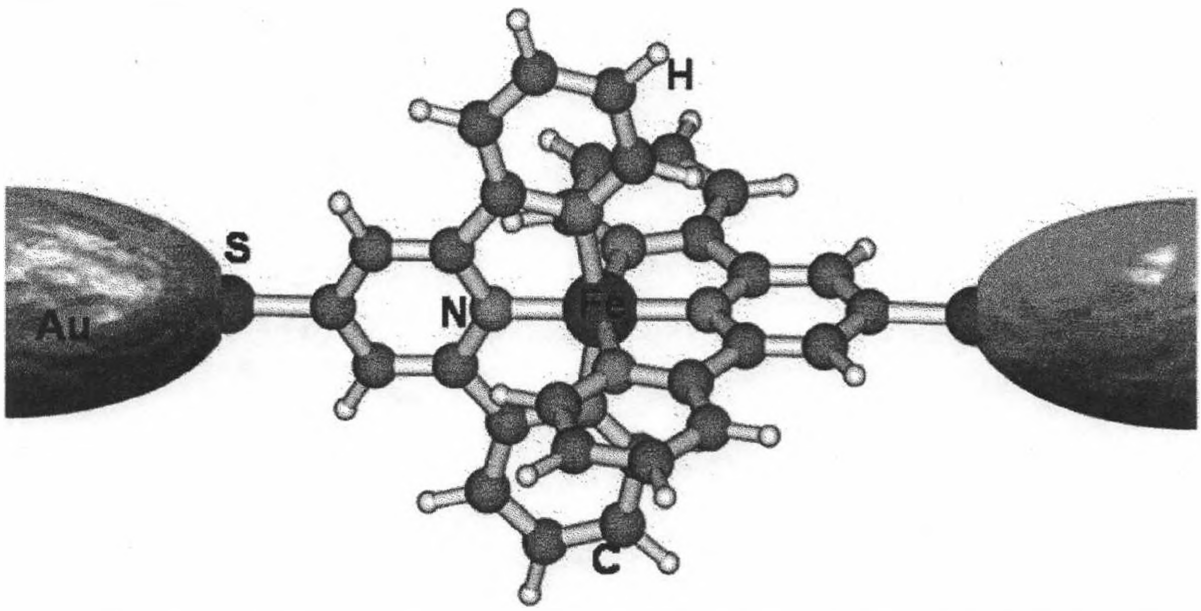

Figure 2.13. (U) Schematic of the strongly coupled Feterpyridine Linker molecule sandwiched between a pair of gold electrodes that can act as a molecular switch[120]

[119] (U) Chen, J., M.A. Reed, A.M. Rawlett, J.M. Tour, "Large On-Off Ratios and Negative Differential Resistance in a Molecular Electronic Device," *Science*, **286**(5444), 1550-1552 (19 November 1999) [doi:10.1126/science.286.5444.1550]

[120] (U) Pati, R., M. McClain, and A. Bandyopadhyay, "Origin of Negative Differential Resistance in a Strongly Coupled Single Molecule-Metal Junction Device," *Phys. Rev. Lett.*, **100**, 246801(4) (20 June 2008) [doi:10.1103/PhysRevLett.100.246801]

(U) Another approach to creating a molecular switch is to attach light-sensitive organic molecules to metal surfaces where they can be switched between two different configurations in response to exposure to different wavelengths of light. Because the configuration changes are reversible and can be controlled without direct contact, this technique could enable applications that can be controlled at the molecular

scale and has been suggested as a possible basis for molecular motors, artificial muscles, and molecular electronics. Progress was impeded however since when such molecules were attached to surfaces, they no longer could be switched back and forth, as they could be when they were in solution.

(U) Kumar *et al.*[121] have developed a new technique that uses a change in the shape of an azobenzene molecule in response to light to provide two different states. The azobenzene molecule consists of a bridge of two nitrogen atoms attached to one another by a double bond, with each nitrogen atom also bound to a benzene ring. The two benzene rings can be on the same side of the molecule (cis configuration) or on opposite sides (trans configuration). When the molecule absorbs energy, in the form of light, it can change between cis and trans configurations in a process called photoisomerization.

(U) The photoisomerization of azobenzene is understood well in solution, but the molecule must be attached to a surface in order to provide a useful molecular switch. Previous attempts to accomplish the switching with attached molecules were unsuccessful, either due to interactions between the molecule and the surface to which it was attached or to interferences between adjacent molecules. A carefully designed tether was used to isolate the functional molecules from one another and from the metal surface. The tethered molecules in the surrounding matrix were isolated on a self-assembled monolayer and this isolation was confirmed using molecular-resolution scanning tunneling microscopy. When the tethered molecules were exposed to ultraviolet light in a specially built scanning tunneling microscope, they switched from the trans to the more-compact cis state. This switch was confirmed by an apparent decrease in height of the molecule above the surrounding surface. The researchers further found that exposure to visible light caused a transition back to the more-extended trans state.

(U) Although an advance, this is just the first step in designing a device that can be driven or actuated by such molecular change. In order to perform useful work as a switch , it will be necessary to coordinate the motion of multiple molecules and to build moving parts into some sort of assembly.

2.8 (U) Directed Self Assembly

(U) Kumar *et al.*[122] have developed a method to directly imprint features as small as 13 nm onto bulk metallic glass (BMG) using thermoplastic forming of the BMG and a favorable wetting behavior. The authors believe the technique enables a reliable and economic process for nanoimprint lithography (NIL). Furthermore, as opposed to other material/technology solutions it provides a solution for both mold (template) and imprint material which makes it particularly interesting for high density data storage. The bulk metallic glasses used to form the nanoscale molds were stronger and more durable than metals or

[121] (U) Kumar, A.S., T. Ye, T. Takami, B.-C. Yu, A.K. Flatt, J.M. Tour, and P.S. Weiss. "Reversible Photo-Switching of Single Azobenzene Molecules in Controlled Nanoscale Environments." *Nano Lett.* **8**(6), 1644-1648 (June 2008) [doi:10.1021/nl080323+]

[122] (U) Kumar, G., H.X. Tang, and J. Schroers. "Nanomoulding with amorphous metals." *Nature*, **457**, 868-872 (12 February 2009) [doi:10.1038/nature07718]

silicon and required fewer lithographic steps. The researchers expect that even finer detail will be possible since the BMGs are only limited by the size of a single atom.

(U) Among the many different types of self-assembled materials, block copolymers (BCPs) have attracted significant interest. They consist of chemically distinct polymer chains (blocks) joined by a covalent bond. The immiscibility of the blocks drives their segregation, but their connectivity prevents complete separation, resulting in pattern formation on the length scale of the blocks (~10 nm). Spheres, cylinders, bicontinuous, or lamellar structures can form depending on the volumetric ratio of the two blocks.[123] The BCPs pattern the resulting array down to the molecular level, offering a precision unattainable by traditional lithography-based methods alone and even correcting irregularities in the underlying chemical pattern. Such nanoscale control also allows the researchers to create higher resolution arrays capable of holding more information than those produced today. Bita *et al.*[124] describe a topographical graphoepitaxy (see Figure 2.14, left) technique for controlling the self-assembly of BCP thin films that produces 2D periodic nanostructures with a precisely determined orientation and long-range order. This work, done in collaboration with Hitachi, is very well-suited for designing hard drives and other data-storage devices, which need uniformly patterned templates—exactly the types of arrangements the block copolymers form most readily. With additional advances, the approach may also be useful for designing more complex patterns such as microchips.

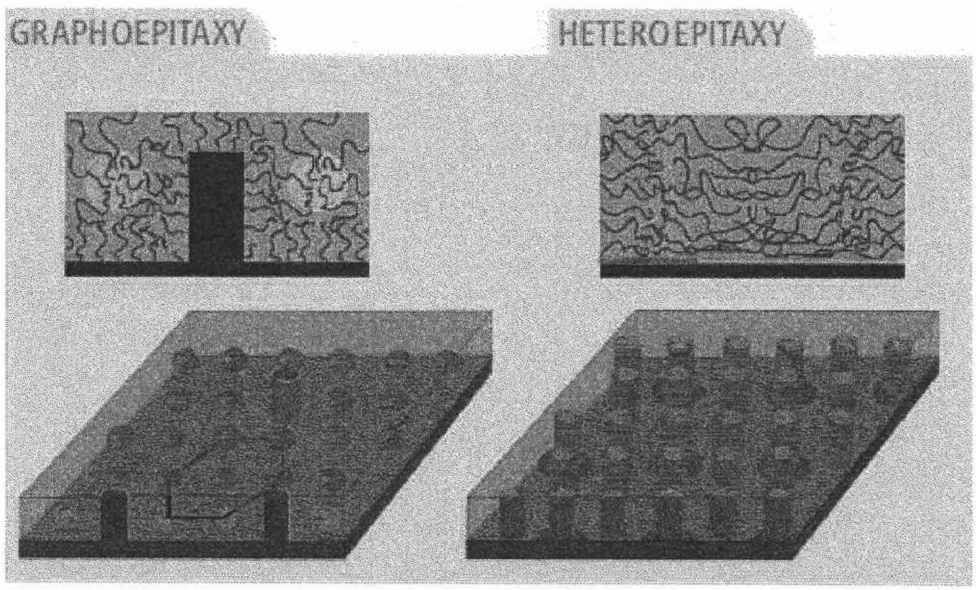

Figure 2.14. (U) Block copolymers self-assemble into regularly sized and spaced nanodomains. Graphoepitaxy (left) and heteroepitaxy (right) create long-range order with templates prepatterned on a length scale greater than the natural lattice of block co-polymer

[123] (U) Segalman, R.A., "Directing Self-Assembly Toward Perfection," *Science*, **321**, 919-920 (15 August 2008) [doi:10.1126/science.1162907]
[124] (U) Bita, I., J.K.W. Yang, Y.S. Jung, C.A. Ross, E.L. Thomas, and K.K. Berggren, "Graphoepitaxy of Self-Assembled Block Copolymers on Two-Dimensional Periodic Patterned Templates," *Science*, **321**, 939-943 (15 August 2008) [doi:10.1126/science.1159352]

(U) A BCP tin film can be used as a template for patterning hard inorganic materials, such as metal nanoparticles. Russell *et al.*[125] used faceted surfaces of commercially available sapphire wafers to guide the self-assembly of block copolymer microdomain s into oriented arrays with quasi–long-range crystalline order over arbitrarily large wafer surfaces. Ordered arrays of cylindrical microdomains 3 nanometers in diameter, with areal densities in excess of 10 terabits per square inch. were produced. The sawtoothed substrate topography provides directional guidance to the self-assembly of the BCP, which is tolerant of surface defects, such as dislocations. The lateral ordering and lattice orientation of the single-grain arrays of microdomains are maintained over the entire surface. Ruiz *et al.*[126] also demonstrated assembly of defect-free arrays of isolated BCP domains at densities up to 1 terabit per square inch on chemically patterned surfaces. An electron beam was used to write a pattern of round spots onto a surface layer, and then the polymer is self-assembled on top of the chemically prepatterned substrate (see Figure 2.14, right).

(U) BCP films are promising candidates for the generation of ultrahigh-density media that have the potential of being addressable. The results suggest exciting routes toward nanopatterns with perfected long-range positional order that are suitable for microelectronic applications. Clearly, the challenge ahead for BCP lithography is to stretch these sparse templating approaches away from expensive, difficult to scale electron beam patterned substrates toward less expensive, scalable options such as optical lithography or other routes that allow the electron beam template to be reused.

(U) Application specific self assembly is also a common theme. Electromagnetic waves at the surface of a metal have the enormous bandwidth of a light pulse and can be channeled into circuit components smaller than the diffraction limit. Such plasmons (quantized light and sound waves) have generated significant interest.[127] Metal nanostructures that support surface plasmons are compelling as plasmonic circuit elements and as the building blocks for metamaterials according to Tao *et al.*[128] They have demonstrated the spontaneous self-assembly of shaped silver nanoparticles into three-dimensional plasmonic crystals that display a frequency-selective response in the visible wavelengths. Extensive long-range order mediated by exceptional colloid monodispersity gives rise to optical passbands that can be tuned by particle volume fraction. These metallic supercrystals present a new paradigm for the fabrication of plasmonic materials, delivering a functional, tunable, completely bottom-up optical element that can be constructed on a massively parallel scale without lithography.

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[125] (U) Park, S., D.H. Lee, J. Xu, B. Kim, S.W. Hong, U. Jeong, T. Xu, and T.P. Russell, "Macroscopic 10-Terabit–per–Square-Inch Arrays from Block Copolymers with Lateral Order," *Science*, **323**(5917), 1030-1033 20 February 2009) [doi:10.1126/science.1168108]

[126] (U) Ruiz, R., H. Kang, F.A. Detcheverry, E. Dobisz, DS. Kercher, T.R. Albrecht, J.J. de Pablo,and P.F. Nealey, "Density Multiplication and Improved Lithography by Directed Block Copolymer Assembly," *Science*, **321**, 936-939 (15 August 2008) [doi:10.1126/science.1157626]

[127] (U) Ebbesen, T.W., C. Genet, and S.I. Bozhevolnyi, "Surface-plasmon circuitry," *Physics Today*, **61**(5), 44-50 (May 2008) [doi:10.1063/1.2930735]

[128] (U) Tao, A.R., D.P. Ceperley, P. Sinsermsuksakul, A.R. Neureuther, and P. Yang, "Self-Organized Silver Nanoparticles for Three-Dimensional Plasmonic Crystals," *Nano Lett.*, **8**(11), 4033-4038 (18 October 2008) [doi:10.1021/nl802877h]

2.9 (U) Spin Materials

(U) Fast memory chips such as DRAMs and SRAMs (Dynamic and Static Random Access Memory) commonly used today are volatile: in case of power interruption, they lose their stored information. Non-volatile forms of semiconductor memory such as flash memory, commonly used in USB drives and in cameras, PDAs, and cell phones, are not very fast and have other problems that have kept them from use in high-performance memory systems, at least at the upper levels of the memory hierarchy. A number of systems are competing to displace flash as the non-volatile memory of choice. Among these are phase-change memory, also known as PRAM, PCM, PCRAM, etc. and perhaps the leading contender, which switches between two states, crystalline and amorphous, with the application of heat to a special glass; programmable metallization cell memory (PMC); Resistive Random Access Memory (RRAM); Nano-RAM, or NRAM, a proprietary technology using carbon nanotubes; and Silicon-Oxide-Nitride-Oxide-Sili con memory (SONOS), a variation of flash. PRAM is potentially fast and can manipulate individual bits, unlike flash, but there are issues with the fact that it is a thermally driven process rather than an electronic one.

(U) Magnetic memory chips called MRAMs (Magnetic Random Access Memory) are also strong contenders for the non-volatile market. In MRAM the digital information is not stored by means of electric charge but by means of the orientation of the magnetization of a magnetic cell, which is determined by the orientation of the electron spin. These devices use spin materials and are sometimes referred to as spintronics devices. Spintronics and molecular electronics manipulate spins and charges in electronic devices and result is such molecular devices as molecular spin-transistors and spin-valves. One of the attractions of these devices is that switching spin orientations may require less energy than is needed to turn a charge current on and off.

(U) The most prominent example of harnessing spin currents is the giant magnetoresistance (GMR) effect, which occurs when electrical current flows through two thin ferromagnetic layers separated by a nonmagnetic spacer layer. When the magnetic domains of the ferromagnetic layers have parallel orientation, current flows more readily than when they are antiparallel, because the current of only one spin type (spin down, for example) undergoes extensive scattering. GMR has found numerous technological applications, including read heads in hard-disk drives, magnetic sensors, and magnetic random-access memory (MRAM). In many of these applications, the metallic spacer layer is replaced by a tunnel barrier made of oxides such as MgO. The associated resistance changes in such tunneling magnetoresistance (TMR) devices can be much greater than those in GMR devices. Less well understood is colossal magnetoresistance (CMR), where materials such as manganese-based perovskite oxides can dramatically change their electrical resistance by orders of magnitude in the presence of a magnetic field.

(U) In today's MRAM devices, spin currents are used only in the reading step through the GMR or TMR effects. In the writing step, the orientation of one of the ferromagnetic layers is changed by applying an external magnetic field. In a new generation of MRAM under development, spin currents are also used to write the bits.[129] When a current passes through the spacer layer, the transport of angular

[129] (U) Katine, J.A., E. E. Fullerton, "Device implications of spin-transfer torques," *J. Magn. Magn. Mater.* **320**(7), 1217-1226 (April 2008) [doi:10.1016/j.jmmm.2007.12.013]

momentum accompanying the spin current provides a spin transfer torque[130] that drives switching of one of the magnetic layers, performing the writing step. Using spin torque the memory state of the cell can be programmed in a very simple way just by applying a current pulse: a positive current switches the magnetization to one direction and a negative current to the other. Spin torque MRAM further promise a high storage density comparable to DRAM and flash, but even if MRAM could be scaled as far as conceivable with advanced lithographic fabrication methods, it will not approach the storage density available in hard-disk drives.[131] Most major semiconductor chip producers are developing spin torque memories.

(U) A spin torque current pulse excites a precessional motion of the magnetization of the memory cell. Normally, the magnetization has to undergo several precessional turns before reliable magnetization reversal takes place requiring present spin torque MRAM prototypes to operate with rather long write pulses of about 10 nanoseconds duration, which limits the MRAM clock speed. Spin torque switching of a nanomagnet as fast as the fundamental speed limit allows, a single precessional turn using ballistic switching, has been recently achieved.[132] This allows non-volatile magnetic memories to operate as fast as the fastest non-volatile memories. It was achieved by precise tailoring of the current pulse parameters in combination with a small magnetic bias field.

(U) Using ballistic spin torque reversal future MRAM could be programmed by current pulses shorter than 1 nanosecond corresponding to write clock rates well above 1 GHz. It could thus enable a high-density and non-volatile memory operating at the clock rates of the fastest volatile memories.

(U) In MRAM applications, spin transfer torques act across a spacer layer; they also act within a single material and can be used to move the pattern of magnetic domain walls (which separate regions of opposite magnetic orientation) along a wire. A proposed "racetrack memory"[133,134] developed at the IBM Almaden Research Center, based on moving domain walls by spin current, would compete with or exceed the memory density of mechanical hard-disk drives. These solid-state devices would stack bits on top of each other, storing information in the magnetic domains, regions of aligned spins, in vertically continuous magnetic wires. Similar to magnetic recording tape, bits of information represented by domain walls would be moved past a device that can read and write the information.

(U) Unlike the tape, however, the magnetic racetrack wires are stationary. The magnetic information is moved by a spin current passing through the wire; so that the pattern of domains moves as the domain walls are carried "downstream" in the spin current. One difficulty in developing such devices has been characterizing the interaction between the spin-polarized current and the magnetic bits.

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[130] (U) Ralph, D.C. and M.D. Stiles. "Spin transfer torques," *J. Magn. Magn. Mater.* **320**(7), 1190-1216 (April 2008) [doi:10.1016/j.jmmm.2007.12.019]

[131] (U) McMichael, R.D. and M.D. Stiles. "A New Spin on the Doppler Effect." *Science*, **322**(5900) 386-387 (17 October 2008) [doi:10.1126/science.1165717]

[132] (U) Serrano-Guisan, S., K. Rott, G. Reiss, J. Langer, B. Ocker, and H.W. Schumacher, "Biased Quasiballistic Spin Torque Magnetization Reversal," *Phys. Rev. Lett.*, **101**(8), 87201(4) (22 August 2008) [doi:10.1103/PhysRevLett.101.087201].

[133] (U) Parkin, S.S.P., M. Hayashi, and L. Thomas, "Magnetic Domain-Wall Racetrack Memory," *Science*, **320**(5873), 190-194 (11 April 2008) [doi:10.1126/science.1145799]

[134] (U) Hayashi, M., L. Thomas, R. Moriya, C. Rettner, S.S.P. Parkin, "Current-Controlled Magnetic Domain-Wall Nanowire Shift Register," *Science*, **320**(5873), 209-211 (11 April 2008) [doi:10.1126/science.1154587]

(U) Using spin to store information is one thing, but manipulating it with logic devices is another. As the ITRS roadmap notes, further understanding of the mechanisms and physical principles will be necessary. Direct measurements of the spin current are challenging, and the properties of the spin current are more often inferred from measurements of the magnetization or the electrical current. Some of the most interesting experiments are those that measure the current-induced motion of a domain wall. This motion is the basis for the racetrack memory mentioned above. One of the difficulties in interpreting these experiments is that unintentional inhomogeneities in the wires also influence the motion of domain walls.[135] Thus, a basic property of the spin current, its polarization--the degree to which the current is carried by either spin-up or spin-down electrons--is not well known, and estimates generally depend on the experimental technique and the fabrication method. Because the polarization is often treated as a free parameter in the analysis of experiments, reliable polarization measurements would constrain experimental analysis and allow deeper understanding of the results.

(U) Vlaminck and Bailleul[136] introduce a reliable method for measuring the spin current polarization that makes use of a novel version of the Doppler effect. They measured the change in the oscillation frequency of spin waves of a fixed wavelength in the presence of the current flow. They use the measured change to determine the effective flow rate of the magnetic medium in which the spin wave propagates. This flow rate is one of the fundamental quantities that characterize current-induced domain wall motion. This experiment is likely to be the first of a series that will enable the measurement of the spin characteristics of currents in ferromagnets. Such studies should also allow for a more quantitative analysis of experiments performed in the development of spin-based devices.

(U) Today, a spin transistor would require a room-temperature magnetic semiconductor but all the true magnetic semiconductors to date have been limited to cryogenic temperatures. Breaking the process down into three stages--spin detection, signal amplification, and spin filtering of that amplified signal--Acremann *et al.*[137] suggest an alternative method that may provide a spin amplifier using a sequence of electrical and magnetic field pulses to manipulate the magnetization of a patterned ferromagnetic layer. Such an engineered spin amplifier using presently available materials may accelerate the development of spintronics, and with it the additional functionality of having sensing, memory storage, and logical operation in a single device.

(U) The ability to manipulate individual spins is also being driven by interest in quantum information processing. Most schemes require fast single-qubit operations. For spin-based qubits, this involves performing arbitrary coherent rotations of the spin state on time scales much faster than the spin coherence time. Although electrical control of a single spin has been achieved, the nanosecond time scales required for such manipulation limit the number of operations that can be performed within the

[135] (U) Beach, G.S.D., M. Tsoi, and J.L. Erskine, "Currrent-induced domain wall motion," *J. Magn. Magn. Mater.* **320**(7), 1272-1281 (April 2008) [doi:10.1016/j.jmmm.2007.12.021]
[136] (U) Vlaminck, V. and M. Bailleul, "Current-Induced Spin-Wave Doppler Shift," *Science*, **322**, 410-413 (17 October 2008) [DOI:10.1126/science.1162843]
[137] (U) Acremann, Y., X.W. Yu, A.A. Tulapurkar, A. Scherz, V. Chembrolu, J.A. Katine, M.J. Carey, H.C. Siegmann, and J. Stöhr, "An amplifier concept for spintronics," *Appl. Phys. Lett.*, **93**(10), 102513(3) (12 September 2008) [doi:10.1063/1.2977964]

spin coherence time. By applying off-resonant, picosecond-scale optical pulses, Berezovsky *et al.*[138] have demonstrated the coherent rotation of a single electron spin through arbitrary angles up to π radians.

2.10 (U) Complex Metal Oxides

(U) According to a recent review,[139] "crystalline oxides can exhibit nearly every possible effect seen in solid-state physics, including magnetism and superconductivity. An even richer spectrum of possibilities becomes available if thin films of different crystalline oxides are combined layer by layer to create artificially structured, heterogeneous materials. The study of these engineered materials is just beginning, but an emerging theme is that the interface between different oxide layers plays a crucial role because it provides an avenue for the study and control of solid-state phenomena at the nanoscale."

(U) These developments are the result of the intrinsic ability of oxides to form heterostructures, coupled with methods for fabricating and characterizing these structures with atomic-layer sensitivity and control. Epitaxial growth--growing a single crystal on top of another--requires a close match of the sizes of the crystal lattices. Heterogeneous metal oxide films lend themselves to epitaxial growth because, despite having different cations, they often share a common sublattice of oxygen atoms. The degree of crystalline perfection now possible in oxide film synthesis rivals that attained in semiconducting systems.

(U) Creating complex metal oxide structures directly on silicon would be of significant importance to many electronics applications, but this has been difficult to achieve due to the structural and chemical difference between silicon and the crystal oxides. Nevertheless, a handful of crystal oxides that display unexpected phenomena at interfaces have been successfully developed on silicon (see the next section on Interfaces).

(U) The possible variety of materials and interfaces is huge to theoretical guidance is important. First-principles electronic structure calculations deal fairly well with the electronic ground states of complex metal oxides. More complicated interactions involving strong electron correlation and spin coupling pose significant challenges to realistic simulations as do realistic representations of impurities. Theorists, nonetheless, have motivated experimentalists to use strain, composition and other tunable external control parameters to optimize and control ferroelecticity in novel oxide systems and have begun to make predictions for novel interfacial properties.

(U) An example of such theory-driven research resulted in the demonstration of ferroelectric functionality in intimate contact with silicon.[140] Guided by predictions[141] made ten years ago, strained

[138] (U) Berezovsky, J., M.H. Mikkelsen, N.G. Stoltz, L.A. Coldren, and D.D. Awschalom, "Picosecond Coherent Optical Manipulation of a Single Electron Spin in a Quantum Dot," *Science*, **320**(5874), 349-352 (18 April 2008) [doi:10.1126/science.1154798]

[139] (U) Reiner, J.W., F.J. Walker and C.H. Ahn, "Atomically Engineered Oxide Interfaces," *Science*, **323**(5917), 1018-1019 (20 February 2009) [doi:10.1126/science.1169058]

[140] (U) Warusawithana, M.P., C. Cen, C.R. Sleasman, J.C. Woicik, Y. Li, L.F. Kourkoutis, J.A. Klug, H. Li, P. Ryan, L.-P. Wang, M. Bedzyk, D.A. Muller, L.-Q. Chen, J. Levy, and D.G. Schlom, "A Ferroelectric Oxide Made Directly on Silicon," *Science*, 324(5924), 367-370 (17 April 2009) [doi:10.1126/science.1169678]

strontium titanate ($SrTiO_3$) was grown epitaxially on silicon and stable ferroelectric nanodomains were observed at temperatures as high as 400 Kelvin. This appears to be a significant step towards a functioning ferroelectric transistor that can switch between nonvolatile memory states using very little power. Still, while guided by theory, there were quantitative differences between experiment and theory that suggest processes that need to be included in the theory.

(U) The application of these materials to areas such as sensors and energy harvesting are likely to precede their use in electronics, first in memory then in logic devices, but as the relationships between structure and behavior become more fully understood, progress in their use in electronics will accelerate.

2.11 (U) Interfaces and Heterointerfaces

(U) As discussed in the previous section, thin film sandwiches of complex metal oxides can display unexpected phenomena at materials interfaces. One example is the interface between lanthanum aluminate ($LaAlO_3$) and strontium titanate ($SrTiO_3$). Both materials are ordinary band insulators, but, with the right number of $LaAlO_3$ layers, a metallic state forms at the nanoscale interface. Furthermore, at *very* low temperatures (0.2 Kelvin), the interface is superconducting. [142] The interesting aspect is that the metallic behavior can be turned on and off in specific regions of the interface by applying a voltage. Using an atomic force microscope tip to apply the voltage, tunnel junctions and field-effect transistors can be created with characteristic dimensions as small as two nanometers. These devices can be modified or erased using the SketchFET [143] on-demand nanoelectronics fabrication platform developed at the University of Pittsburgh.

2.12 (U) Modeling and Simulation

(U) Although there have been considerable successes using simulations of various models such as tight binding, where it is assumed that the Fourier transform of the Bloch function can be approximated by a linear combination of atomic orbitals, or the somewhat simpler Hubbard [144] model that uses a two-term Hamiltonian where the kinetic energy term allows tunneling, there is much room for improvement. Relativistic effects, spin-orbit coupling, electron-electron interactions and impurities represent some of the computational challenges facing device physics today.

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[141] (U) Robertson, J. and C.W. Chen, "Schottky barrier heights of tantalum oxide, barium strontium titanate, lead titanate, and strontium bismuth tantalite." *Appl. Phys. Lett.* **74**(8), 1168-1170, (22 February 1999) [doi:10.1063/1.123476]

[142] (U) Reyren, N., S. Thiel, A. D. Caviglia, L. Fitting Kourkoutis, G. Hammerl, C. Richter, C. W. Schneider, T. Kopp, A.-S. Rüetschi, D. Jaccard, M. Gabay, D. A. Muller, J.-M. Triscone, J. Mannhart, "Superconducting Interfaces Between Insulating Oxides." *Science*, **317**(5842), 1196-1199 (31 August 2007) [doi:10.1126/science.1146006]

[143] (U) Cen, C., S. Thiel, J. Mannhart, and J. Levy, "Oxide Nanoelectronics on Demand," *Science*, **323**(5917), 1026-1030 (20 February 2009) [doi:10.1126/science.1168294]

[144] (U) Hubbard, J., "Electron Correlations in Narrow Energy Bands." *Proc. Roy. Soc. A*, **276**(1365) 238-257 (26 November 1963) [doi:10.1098/rspa.1963.0204]

(U) Consider the computational effort that won the 2008 Gordon Bell award.[145] Using the DCA++ code, which implements a Dynamical Cluster Approximation [146] in conjunction with the Hirsch-Fye Quantum Monte Carlo algorithm [147] in the context of a microscopic two-dimensional Hubbard model, the authors studied the effect of disorder and nano-scale inhomogeneities on the pair-formation and the superconducting transition temperature of real cuprates (copper oxide separated by layers of insulating material). The award-winning run achieved a sustained performance of 1.352 petaflops (mixed single and double precision).

(U) Sean Hartnol [148] has pointed out some intriguing possible uses for string theory in the context of device physics.

(U) String theory was first formulated in the early 1970s with the objective of explaining aspects of the strong interactions of particle physics. The strings were literally strings of energy that bound together a quark and an antiquark to form subatomic particles called mesons. This original string theory, however, was ultimately unsuccessful and it was only consistent in 10 dimensions of spacetime. String theory was then reincarnated as a unifying theory of quantum gravity, with breakthroughs in the mid-1980s ushering this grander version into the mainstream. A recent turn of events is leading a growing fraction of string theory research back to studying specific laboratory systems, including those of *condensed matter physics*.

(U) This shift has been possible due to recent developments in the mathematical construct known as the holographic correspondence. Also known as the anti-de Sitter/conformal field theory correspondence (or AdS/CFT for short),[149] it relates Einstein's general theory of relativity to quantum mechanics. It asserts that string theory in 10 or 11 dimensions may be equivalent to a distinct theory in the four space-time dimensions in which we live. This correspondence is called holographic by analogy to a hologram, in which a three-dimensional image is stored on a two-dimensional surface. Through the holographic correspondence, the many dimensions of string theory are encoded in a lower-dimensional theory that appears not to have anything to do with strings at all. Instead, this lower-dimensional theory shares many features with exotic theories that describe *electrons in materials* at so-called quantum critical points.[150]

(U) Quantum critical systems and the holographically repacked string theory share the feature of scale invariance, whereby the system responds in the same way at whatever energy scale or distance scale it is probed. An example of quantum criticality arises in the superconducting-to-insulator transition seen in

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[145] (U) Alvarez, G., M.S. Summers, D.E. Maxwell, M. Eisenbach, J.S. Meredith, J.M. Larkin, J. Levesque, T.A. Maier, P.R.C. Kent, E.F. D'Azevedo, and T.C. Schulthess, "New algorithm to enable 400+ TFlop/s sustained performance in simulations of disorder effects in high-T_c superconductors," *Proceedings of the 2008 ACM/IEEE conference on Supercomputing*, Austin, (15-21 November 2008) [doi:/doi.acm.org/10.1145/1413370.1413.433]

[146] (U) Maier, T., M. Jarrell, T. Pruschke, and M.H. Hettler, "Quantum cluster theories," *Rev. Mod. Phys.* **77**, 1027-1080, (July 2005) [doi:10.1103/RevModPhys.77.1027]

[147] (U) Hirsch, J.E., R.M. Fye, "Monte Carlo Method for Magnetic Impurities in Metals," *Phys. Rev. Lett.*, **56**(23), 2521-2524 (9 June 1986) [doi:10.1103/PhysRevLett.56.2521]

[148] (U) Hartnol, S., "Stringing Together a Solid State," *Science*, **322**(5908), 1639 – 1640 (12 December 2008) [doi:10.1126/science.1166668]

[149] (U) Taubes, G., "String Theorists find a Rosetta Stone," *Science*, **285**(5427), 512-517 (3 July 1999) [doi:10.1126/science.285.5427.512]

[150] (U) Sachdev, S., "Quantum magnetism and criticality," *Nature Physics*, **4**, 173 - 185 (01 Mar 2008) [doi:10.1038/nphys894]

thin films at zero temperature as the thickness of the film is varied.[151] Precisely at the quantum critical point, the film is neither superconducting nor perfectly insulating but instead has a universal finite resistivity. The scale invariance of quantum critical systems makes them difficult to study using the traditional tool kit of condensed matter physics. This is because the electrons are strongly correlated and cannot be treated as individual particles weakly interacting with each other. Furthermore, the absence of a preferred scale means that approximations for low-energy or high-energy processes cannot be made. Because quantum critical behavior has been observed in many systems and is believed to play a role in important processes such as high-temperature superconductivity,[152] it is therefore necessary to overcome these difficulties.

(U) The immediate consequence of the holographic correspondence is that there is a different description, a "dual" description, of the condensed matter system in terms of higher-dimensional string theory. Certain questions actually turn out to be easier to address using the dual method. One reason is that scale invariance is built into the string theory description from the start. Another is that, whereas the original system was highly quantum mechanical, the dual description can be purely classical.

(U) Several recent works have used string theory techniques to attack condensed matter problems involving quantum critical transport.[153,154] From a theoretical description of the flow of electric and heat currents in systems that are close to quantum criticality, it was possible to predict a "hydrodynamic cyclotron resonance" for a charged quantum critical system in the presence of an external magnetic field.[155] This resonance has certain characteristic features—for instance, its width is related to the universal conductivity at the critical point—and may be observable in future measurements on graphene.[156]

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[151] (U) Goldman, A. and N. Markovi ć, Superconductor-Insulator Transitions in the Two-Dimensional Limit," *Physics Today*, **51**(11), 39-44 (November 1998) [doi:10.1063/1.882069]

[152] (U) Sachdev, S., "Order and quantum phase transitions in the cuprate superconductors," *Rev. Mod. Phys.*, **75**(3), 913-932 (16 July 2003) [doi:10.1103/RevModPhys.75.913]

[153] (U) Herzog, C.P., P. Kovtun, S. Sachdev, and D.T. Son, "Quantum critical transport, duality, and M theory," *Phys. Rev. D*, **75**(8), 085020(20), (27 April 2007) [doi:10.1103/PhysRevD.75.085020]

[154] (U) Hartnoll, S.A., P.K. Kovtun, M. Müller, S. Sachdev, "Theory of the Nernst effect near quantum phase transitions in condensed matter and in dyonic black holes," *Phys. Rev. B*, **76**(14), 144502(23), (4 October 2007) [doi:10.1103/PhysRevB.76.144502]

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3.0 (U) Scenarios

(U) In the background section we have presented a brief overview of where things stand today. Future progress in holding to Moore's Law is in doubt because of the apparent end of scaling for CMOS technology. The two main sources of doubt are the end of Dennard scaling for CMOS and the barriers to lithographic scaling in getting to nanoscale devices. This is not the first time the future of Moore's Law has been in doubt and no one is predicting the collapse of the silicon-based semiconductor industry, but the path forward is not a clear as it once was.

(U) The challenge of putting more, smaller devices on a chip is, of course, only one piece of the larger effort to address critical problems using information technology. Other problems include moving enough data on and off the chip as well as powering and cooling it. Integrating thousands or millions or more chips into a useable, functioning, reliable system are further problems outside the scope of this report.

(U) This report considers two scenarios that offer the potential of keeping Moore's Law on track in the future. The first is carbon-based nanoelectronics and the second involves the use of complex metal oxides. A third scenario considers what would happen if Moore's Law does indeed slow significantly and even stops.

3.1 (U) Scenario 1: Carbon-Based Nanoelectronics

(U) Carbon-based semiconductors are poised to eventually take over the role played by silicon. This will not happen all at once or very soon. Graphene and single walled carbon nanotube (SWCNT)-based devices will initially appear in special purpose devices, where their unique characteristics offer a special advantage, in conjunction with all the other materials that form the backbone of today's electronic industry. Although SWCNTs have been around longer, they are harder to work with than graphene, so interest in them for electronics is likely to shrink as graphene becomes a commodity item, except where nanotubes offer benefits (optical waveguides, optical-electrical interfaces?) not matched by graphene. As experience is developed and manufacturing processes smoothed out, a larger and larger proportion of a chip will be carbon based instead of silicon. When device sizes drop below ten nanometers, carbon will be the dominant material.

(U) It seems possible that carbon-based electronics will put us back on the Moore's Law curve that has been historically experienced, but by 2030 it is likely that nearly all the capability of a two-dimensional system will have been exploited. At that point expect a move to vertically connect a stack of 2D systems. A number of possibilities suggest themselves: using nanotubes as vertical pipes to connect successive layers; nanoribbons connecting the edges of vertically arranged graphene layers; graphene sheets folded back onto themselves like a stack of towels; graphene sheets wound around an axis. At that point the doubling quantity becomes the number of layers. Assuming the starting point is a 100 nm layer, 10^5 layers only occupy 1 cm. Doubling the number of layers every other year would take another 34 years. In other words, Moore's Law in this scenario could easily go past 2060.

3.2 (U) Scenario 2: Complex Metal Oxides

(U) In a world where silicon maintains its dominance while technology improves at a steady pace, complex metal oxides are likely to play a growing role as enhancers of capability, particularly in areas where spin plays a role. Spin has intrinsically better energy efficiency attributes and holds the promise of fast, non-volatile memory. The challenge will be to displace silicon-based transistors in an area where conventional technology is strongest

(U) Future superconducting devices will depend on theory-driven engineered materials in this class, but there is no indication that this will be accomplished at anywhere near room temperature. Such cryogenic requirements obviously rule out the commodity market and substantially drive up the cost. There have been attempts in the past to exploit the superior performance of low-temperature materials, but they have always been abandoned as they fell behind commodity performance and their inherently more fragile nature raised reliability issues. It is extremely difficult to build large systems at low temperatures and control the necessary thermal gradient requirements throughout. In some respects superconducting computers have aspects in common with ASICs and other special purpose computing hardware such as FPGAs—they take longer to develop, are more expensive and are in danger of being overtaken by commodity devices. That is, of course, unless the progress expressed as Moore's Law dramatically slows, extending the advantage lifetime of the special system.

3.3 (U) Scenario 3: The End of Moore's Law

(U) This scenario considers the consequences and technological implications of Moore's Law not continuing past 2020. The assumption is that it will be economically and/or technologically impractical to go beyond half-pitch sizes of 22 nm, which could have gates as small as 10 nm (about 100 atoms). This would limit the number of transistors per chip to less than 100 billion. In a worst case scenario memory chips would use a different lithographic process than logic chips; perhaps cramming only 50 billion transistors onto a logic chip. This would mean that uniting memory and logic devices to minimize data flow would not be any easier.

(U) At 100 million transistors per complex core, a chip could have 500 cores. With simpler core designs, chips with 4k to 8k cores are conceivable and consistent with doubling the number of cores each generation from now until 2020.

(U) To make use of that many cores on a chip a number of other things have to happen, not the least of which is improving the bandwidth for moving data on, off and within the chip. If integrated optoelectronics becomes available, which seems likely in this time-frame then the bandwidth problem may be manageable. We already have experience programming at this level of parallelism so that should not be a problem, although programming an entire system will continue to be a challenge.

(U) With so many cores power efficiency requirements will restrict the clock frequencies to not much more than what is available today, i.e., a few gigahertz. An optimistic value might be 10 GHz. In that case 500 cores producing 4 ops/clock at 10 GHz would be capable of 20 teraops. A million chip system would have an aggregate peak capability of 20 exaops, appropriate for this time-frame. The more aggressive design with more but simpler cores could easily be a factor of ten higher.

(U) The question was posed whether or not the performance gap between FPGA and ASIC designs will narrow in an environment where Moore's Law is not driving performance increases. One of the reasons commodity processors have had an advantage over FPGA and ASIC designs is that their performance could be expected to increase at a steady rate so that they could eventually overtake the initially superior performance of the FPGA or the even more superior ASIC and be very cost-effective throughout. As ASICS became more complex (and capable) to use the transistors Moore's Law was supplying, the design time and fabrication costs skyrocketed. FPGAs have proved more cost-effective than ASICS of late, but they are much harder to program than commodity processors. In a world where processor chips are not steadily improving in performance, one might expect them to remain permanently behind the capabilities of FPGAs, which would remain behind ASICS. For this to be true the time and cost to develop the more specialized device must remain acceptable and feasible. Will the time it takes to design a 50- or 100-billion transistor ASIC be an acceptable delay over the effort it takes to get a commodity (or FPGA) chip of similar scale producing results? Will the performance of the commodity chip steadily improve through algorithmic changes to the point its performance is within range of the ASIC? The answer is probably yes. Complex devices tend to be more efficient if there is a simpler set of functional units that can be more easily optimized. ASICs can of course be designed with this principle in mind, but as the functional unit becomes more general to handle a range of cases it starts to look like a general-purpose processor.

4.0 (U) Technology Forecast Analysis

(U) Moore's Law is not driven by an abstract compulsion to improve the performance of information technology. It is driven by economics and competition. When a new generation of equipment makes the old version no longer cost-effective, it is possible for new players to get into the game with a better widget. The major semiconductor companies would be quite happy to continue making a profit off their current products and not invest in research and development. In the absence of competition, this is what would happen. Competition exists, however, and it is fierce. The companies know that without R&D investments their competitors will develop products that will take away their business. To help insulate the established industry members from surprises, organizations like ITRS help look ahead and identify areas where progress can be made economically.

(U) The expense of new fabrication facilities has been steadily growing to the point where a company that makes a mistake and invests in the wrong technology can suffer severe financial setbacks and even go out of business. This makes investment in new technologies actually rather conservative. Incremental improvements are safer investments than new technologies requiring new equipment, i.e., the shift from deep UV to EUV, l*et a*lone radical new technologies that have never been demonstrated at scale. Investors with tolerance for risk, i.e., venture capitalists, do fund risky technologies and occasionally score big successes, but the success rate is not high. Still, the opportunity to hit it big is a powerful incentive.

(U) One of the reasons ITRS is so successful is that it operates in the precompetitive area. It identifies feasible processes and challenges that must be overcome. A basic investment in the underlying science and engineering is necessary and the majority of that investment will never come from the industry. Industry research labs primarily focus on the refinements of the technologies developed in universities and national laboratories funded by society at large.

(U) In this forecast the near-term investments are the responsibility of the commercialization component of the semiconductor industry. They are driven by short-term profit considerations and maintaining a competitive edge. The mid-term investments tend to be made by the industry R&D labs that are refining and investigating alternatives for commercialization. The far-term investments are more likely to be made by government agencies funding basic research.

(U) This report takes the position that the most likely scenario is the shift to carbon-based electronics. The probability of carbon having a significant role in the semiconductor industry by 2030 is high, better than 90 percent. Silicon will not disappear if for no other reason than it is a useful substrate. Complex metal oxides will also play a role, but the emphasis will be on spintronics. Complex metal oxide-based spintronics and carbon-based nanoelectronics are both likely to coexist as long as there is no competitive spin-based mechanism available using carbon. Spintronics with carbon is a possibility, but for at least the next ten years, the advantage should remain with the complex metal oxides.

(U) Although there will very likely be periods of slowed growth as technologies transition from one to another, as has happened before, this report sees a very low probability that Moore's Law will slow significantly or come to a halt.

4.1 (U) Near-term

(U) The next three years for the semiconductor industry are pretty well determined. Changes in the industry, particularly significant ones, do not take place that quickly. The shift to using high-κ materials such as hafnium oxide took a full decade from laboratory prototypes to production. CMOS enhanced with a variety of approaches, including high-κ materials and vertical construction, will remain the technology of choice. The major decision is which lithographic technology will be used at 22 nm. Will it be enhanced deep UV or will it be the long anticipated extreme UV. This report believes that deep UV will be the primary technology initially, but EUV systems will be striving to displace them and will eventually succeed. The principal driver for EUV will be logic circuits because deep UV seems capable of meeting the demand for memory devices.

(U) The emerging dichotomy between memory and logic fabs should be of concern to organizations interested in high-performance logic devices. The more regular patterning demands of memory devices are likely to be driven by a new generation of cell phones, PDAs and embedded devices that do not have exceptional computational demands. A trend is already emerging where the design focus is shifting to emphasize simpler, low-power processors for the embedded market. An example is the proposed climate computer based on commodity low-power embedded processors (the Tensilica Xtensa).[1] These chips will use the many-core paradigm to compensate for the lower performance of a single core. Maximum clock speed for the 167-processor AsAP,[2] a chip fabricated by STMicrotronics and designed for signal processing, is 1.2 gigahertz, but at slower speeds its energy efficiency soars. Twelve chips working together could perform more than half-a-trillion operations per second (.52 Teraops/sec), while using less power than a 7-watt light bulb.

(U) In the near term, expect continued characterization of the properties of graphene (and carbon nanotubes) and refinements in techniques for working with these materials. There is much that is not known about the behavior and properties of these fairly exotic and physically interesting materials. Much of the research on graphene is being driven by its unique nano- and nearly macro-scale quantum properties that are much more accessible to observation than any other currently know material. In some respects our understanding of graphene and carbon nanotubes is more like the understanding of silicon fifty years ago. Fifty years of detailed knowledge of the behavior of silicon and its oxides is a considerable advantage that will take some time for carbon-based materials to overcome—but it won't take fifty years. Carbon nanotubes have been under investigation for fifteen years and are still a long ways from playing a key role in semiconductors. Much of the lack of progress can be attributed with the inability to manipulate nanoscale materials of this type—controlling the placement and performance of nanotubes is still more art than engineering. Graphene, on the other hand, should progress more quickly to usable devices as experience in working with it on a larger two-dimensional scale is developed.

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[1] (U) Wehner, M., L. Oliker, and J. Shalf. "Towards Ultra-High Resolution Models of Climate and Weather." *International Journal of High Performance Computing Applications*, **22**(2), 149-165 (May 2008) [doi:10.1177/1094342007085023]

[2] (U) Truong, D.N., W. H.Cheng, T. Mohsenin, Z. Yu, A.T. Jacobson, G. Landge, M.J. Meeuwsen, C. Watnik, A.T. Tran, Z. Xiao, E.W. Work, J.W. Webb, P.V. Mejia, and B.M. Baas. "A 167-Processor Computational Platform in 65 nm CMOS." *IEEE J. Solid-State Circuits*, **44**(4), 1130-1144 (April 2009) [doi:10.1109/JSSC.2009.2013772]

(U) Learning to reliably manipulate the electronic state of graphene at the nanoscale will be the primary objective in the near term. The effort can be divided into several fronts:

- Substrate: which surfaces result in metallic and which yield semiconductor forms of the overlaying graphene? Can the substrate be efficiently patterned at the desired scale? What is the impact of the size of a nanoribbon defined by the substrate?
- Surface deposition: Can the electronic state be reliably manipulated by the controlled deposition of material, *e.g.*, hydrogen atoms, on the surface of the graphene sheet?
- Edge reconstruction: the electronic state of graphene nanoribbons is determined by the carbon atoms on the edge—the spatial configuration (zigzag *vs.* arm-chair), the bond termination and how far apart the edges are—make a big difference. Can these factors be efficiently and reliably controlled?
- Shaping: patterning the graphene sheet itself may be an effective way (in conjunction with the approaches just mentioned) of determining device function and performance. How can this best be accomplished? Dry etching? Electron beam?

(U) These fundamentals need to be addressed before further issues such as interfaces, connection, and information exchange with other on- and off-chip devices can be seriously confronted. Efforts to accelerate these issues are probably premature before the fundamental characteristics and manipulation tools are more developed.

4.2 (U) Mid-term

(U) This time frame, out to four to six years, is a critical period for the semiconductor industry. CMOS will be near the end of its ability to sustain Moore's Law and it is unlikely that any technology, including carbon-based nanoelectronics, will be ready to pick up the slack. Performance will fall further away from the historical trends supporting Moore's Law.

(U) This is the period when integrated optical-electronic products should begin making a performance impact by relieving some of the data bottlenecks that currently constrain processor performance. Silicon-based technology has already demonstrated success in fabricating passive linear optical devices such as filters. Now ultra-fast active silicon-based functionalities, such as all-optical switching, are beginning to appear in the laboratory and should make it into commercial devices in this period. Koos *et al.*,[3] recently used mature CMOS processing to fabricate a waveguide and molecular beam deposition to cover it with organic molecules that efficiently mediate the all-optical interaction without introducing significant absorption. The 4-mm-long waveguide was used in the demultiplexing of a 170.8 Gb/s signal to 42.7 Gb/s using four-wave mixing. They claim it is the fastest silicon photonic optical signal processing demonstrated so far.

(U) For carbon-based electronics, this period will begin showing the benefits of improved material handling and more interesting devices should start appearing in the laboratory. Integration with silicon-based electronics will be the goal rather than outright replacement. The appearance of much

[3] (U) Koos, C., P. Vorreau, T. Vallaitis, P. Dumon, W. Bogerts, R. Baets, B. Esembleson, I. Biaggio, T. Michinobu, F. Diedrigh, W. Freude, and J. Leuthold, "All-optical high-speed signal processing with silicon–organic hybrid slot waveguides," *Nature Photonics*, **3**, 216-219 (April 2009) [doi: 10.1038/nphoton.2009.25]

higher frequency (more than 100 GHz) graphene-based transistors can be expected to start appearing as experimental devices. More complex devices should also start appearing, although not necessarily at the nanoscale. Relatively conventional lithographic technology will be used to make working devices but probably not competitive with CMOS, which will still have considerable momentum and investment driving it. More effort will be put into the interfaces between the carbon world and the rest of the chip.

(U) One of the key aspects of the transition to carbon will be to what extent carbon can use the manufacturing infrastructure built for silicon. If the lithographic processes can be adapted without major changes, then this will speed the adaption of carbon. A commercial lithographic process for carbon above the nanoscale is important to develop experience and a comfort zone for the industry. A shift to carbon that involves a dramatic shift in manufacturing processes is very risky and much less likely to be taken unless the new manufacturing process turns out to be significantly cheaper, which is very unlikely.

4.3 (U) Far-term

(U) It is at least ten years, probably fifteen, before commercial products with any significant carbon-based components appear. It simply takes that long to make the transition to a vastly different technology. It could be another five years after that before the real promise of carbon-based nanoelectronics is finally realized.

(U) What might such a device look like in 2030?

(U) Teraherz transistors seem very realistic, putting the industry back on the Moore's Law performance curve. Assume a feature size of 4 nm is feasible, which is compatible with the anticipated ITRS reduction of 0.7x every three years (but about ten years behind the current doubling every two years). This is likely to be the result of a combination of self-assembled structures and some form of vapor deposition or epitaxial growth and not inconsistent with the 3-nm-diameter structures on 6.9-nm centers mentioned in the background section that suggested densities in excess of ten terabits per square inch. Ten trillion transistors per chip would actually be ahead of the current Moore's Law estimate for 2030. Some additional cleverness in packing and layout would obviously be necessary to make this a reality. Although the number of transistors per processor can vary greatly, a hundred million seems reasonable. So a hundred thousand processors (perhaps a million) per chip is conceivable. A chip with 10^6 processors running at 10^{12} Hertz is capable of over 10^{18} operations per second. Conventional wisdom currently postulates the existence of an exaflop (10^{18}) in 2018 and the next step on that growth curve would be a zettaflop (10^{21}) in 2028, i.e., only a thousand or so graphene superchips a couple years later in 2030.

(U) This may be optimistic of course, but there doesn't seem to be any *fundamental* barriers. Not enough is known about the power budget to say for sure, but the optimistic view is that graphene re-enables Dennard scaling. This is based on a combination of ballistic electrons and quantum confinement. *e.g.*, quantum dots and one- and two-dimensional systems. Quantum confinement does not eliminate tunneling, which remains important, but simulations, based on a non-equilibrium Green's

function approach, indicate that GNR MOSFETS outperform[4] ultrascaled silicon devices in terms of drive current capabilities and control. The simulation also suggested that the tunneling could be effectively exploited in band-to-band tunneling devices. Finally, the inevitable degradation of energy to heat is less worrisome in a carbon-based environment because of its superior thermal conductivity and stability.

[4] (U) Liang, G., N. Neophytou, M.S. Lundstrom, and D. Nikonov, "Ballistic graphene nanoribbon metal-oxide-semiconductor field-effect transistors: A full real-space quantum transport simulation," *J. App. Phys.*, **102**(5), 054307(7) (1 September 2007) [doi:10.1063/1.2775917]

5.0 (U) Analysis of Commercial Adoption/Implementation

(U) The semiconductor industry is expected to be a $260 billion market in 2009, according to a KPMG report.[1] The Semiconductor Industry Association (SIA) says the worldwide sales of semiconductors in 2008 was $249 billion, with the U.S. share $120 billion.[2] The industry is dominated by Taiwan, South Korea, the United States, and Japan. Participation in the ITRS, as shown in Figure 5.1, is another reasonable breakdown of the five leading chip manufacturing regions of the world that shows although not as significant an economic force as the other regions, Europe maintains a considerable research interest.

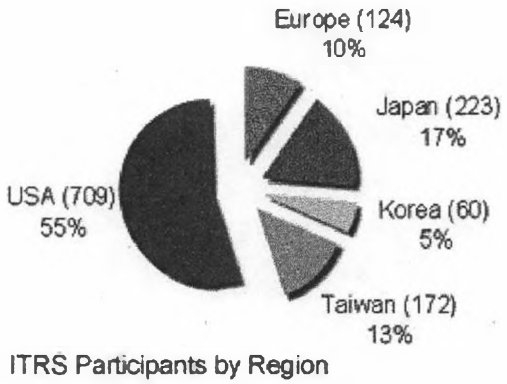

Figure 5.1. (U) ITRS participants by region

(U) The major semiconductor manufacturers, especially Intel and IBM, have significant investments in developing carbon-based electronics. IBM, in particular, has a considerable number of publications from groups at the Watson Research Center. Intel has fewer publications and mostly in association with university partners, both domestic and foreign. A search for "graphene" from the principal corporate websites yielded 43 hits for IBM and 5 for Intel. Many of the IBM hits were different versions of the same piece of research and only two of the Intel hits involved research, one from 2006 and the other 2007. A similar search of Samsung turned up no hits although this report cites work being done by Samsung. NEC had 14 hits, many involving research partners in the United States, including NEC Laboratories America and Columbia University. Sony reported 22 hits, but none of them anything to do with graphene. No hits were obtained for Taiwan Semiconductor Manufacturing Co. (TSMC), Toshiba, STMicroelectronics, Texas Instruments, Renesas (merging operations with NEC), Hynix Semiconductor, NXP Semiconductors, United Microelectronics (UMC), Infineon, or Freescale.

[1] (U) Semiconductor Industry. http://en.wikipedia.org/wiki/Semiconductor_industry

[2] (U) Industry fact sheet. http://www.sia-online.org/cs/industry_resources/industry_fact_sheet

6.0 (U) Research Activities

6.1 (U) National Nanotechnology Initiative

(U) The National Nanotechnology Initiative[1] (NNI) provides a multi-agency framework to ensure U.S. leadership in nanotechnology that will be essential to improve human health, economic well being, and national security. The NNI invests in fundamental research to further understanding of nanoscale phenomena and facilitates technology transfer.

(U) The federal agencies that participate in the National Nanotechnology Initiative under the auspices of the Nanoscale Science, Engineering and Technology (NSET) Subcommittee[2] of the National Science and Technology Council (NSTC)[3] are:

- Department of Commerce (DOC)
  - Bureau of Industry and Security
  - Nanotechnology at National Institute of Standards and Technology (NIST)
- Consumer Product Safety Commission
- Department of Agriculture (USDA)
  - Nanotechnology at Cooperative State Research, Education, and Extension Service (CSREES)
  - Forest Service
- Department of Defense (DoD)
  - Air Force Office of Scientific Research (AFOSR)
  - Army Engineering R&D Center
  - Army Research Laboratory (ARL)
  - Army Research Office (ARO)
  - Defense Advanced Research Projects Agency (DARPA)
  - Defense Research & Engineering (DDR&E)
  - Defense Threat Reduction Agency (DTRA)
  - Office of Naval Research (ONR)
- Intelligence Community
- Department of Education (Ed)

[1] (U) National Nanotechnology Initiative (NNI). http://www.nano.gov/
[2] (U) Nanoscale Science, Engineering and Technology (NSET) Subcommittee. http://www.nano.gov/html/about/n_set.html
[3] (U) National Science and Technology Council (NSTC). http://www.ostp.gov/cs/nstc

- Department of Energy (DOE)
  - Office of Science
    - Office of Basic Energy Sciences (BES)
  - Office of Fossil Energy (FE)
  - Office of Energy Efficiency and Renewable Energy (EERE)
    - Office of Industrial Technologies
- Department of Homeland Security (DHS)
- Department of Justice (USDOJ)
- Department of Labor (DOL)
- Occupational Safety & Health Administration (OSHA)
- Department of State
- Department of Transportation (DOT)
- Department of Treasury
- Environmental Protection Agency
  - Nano Research
  - Nanotechnology under the Toxic Substances Control Act (TOSCA)
- Department of Health and Human Services (DHHS)
  - Nanotechnology at Food and Drug Administration
  - National Institutes of Health
  - Nanotechnology at National Institute for Occupational Safety and Health (NIOSH)
- International Trade Commission
- National Aeronautics and Space Administration (NASA)
- Nanotechnology at the National Science Foundation (NSF)
- Nuclear Regulatory Commission
- Patent and Trademark Office
- US Geological Survey

6.2 (U) DOE Nanoscale Science Research Centers

(U) The DOE's Office of Science Program Office of Basic Energy Sciences (BES), in support of the National Nanotechnology Initiative (NNI) funds these five Nanoscale Science Research Centers (NSRCs) to support the synthesis, processing, fabrication and analysis of materials at the nanoscale:

- Center for Functional Nanomaterials (CFN) at Brookhaven National Laboratory

- Center for Integrated Nanotechnologies (CINT) at Sandia and Los Alamos National Laboratories
- Center for Nanophase Materials Sciences (CINT) at Oak Ridge National Laboratory
- Center for Nanoscale Materials (CNM) at Argonne National Laboratory
- Molecular Foundry (Foundry) at Lawrence Berkeley National Laboratory

(U) These facilities are designed to be the Nation's premier user centers for interdisciplinary research at the nanoscale, serving as the basis for a national program that encompasses new science, new tools, and new computing capabilities. Together, the NSRCs provide a gateway to other major BES user facilities for X-ray, neutron, and electron scattering. Each NSRC contains clean rooms, laboratories for nanofabrication, one-of-a-kind signature instruments, and other instruments (*e.g.*, nanopatterning tools and research-grade probe microscopes).

6.3 (U) National Science Foundation Centers and Networks of Excellence

(U) The National Science Foundation has established the following NNI centers:

6.3.1 (U) Engineering Research Center

- Center for Extreme Ultraviolet Science and Technology
  University of Colorado—Boulder

6.3.2 (U) Science and Technology Center

- Nanobiotechnology Center
  Cornell University

6.3.3 (U) Nanoscale Science and Engineering Centers

- Center for Hierarchical Manufacturing
  University of Massachusetts—Amherst
- Center for Nanoscale Systems (NSEC)
  Cornell University
- Science of Nanoscale Systems and their Device Applications (NSEC)
  Harvard University
- Center for Biological and Environmental Nanotechnology
  Rice University
- Center for Integrated Nanopatterning and Detection (NSEC)
  Northwestern University
- Center for Electronic Transport in Molecular Nanostructures (NSEC)
  Columbia University

- Center for Directed Assembly of Nanostructures (NSEC)
  Rensselaer Polytechnic Institute
- Center for Scalable and Integrated Nano-Manufacturing (NSEC)
  University of California—Los Angeles
- Center for Chemical-Electrical-Mechanical Manufacturing Systems (NSEC)
  University of Illinois, Urbana-Champaign
- Center on Templated Synthesis and Assembly at the Nanoscale
  University of Wisconsin
- Center for Probing the Nanoscale
  Stanford University
- Center for Affordable Nanoengineering of Polymeric Biomedical Devices
  Ohio State University
- Center of Integrated Nanomechanical Systems
  University of California—Berkeley
- Nano-Bio Interface Center
  University of Pennsylvania
- Center for High Rate Nanomanufacturing
  Northeastern University

6.3.4 (U) Materials Research Science and Engineering Centers (MRSECs)

(U) These four MRSECs are fully dedicated to nanotechnology research:

- Center for Nanoscale Science (MRSEC)
  Pennsylvania State University
- Center for Quantum and Spin Phenomena in Nanomagnetic Structures (MRSEC)
  University of Nebraska, Lincoln
- Center for Research on Interface Structure and Phenomena (MRSEC)
  Yale University
- Genetically Engineered Materials (MRSEC)
  University of Washington

(U) In addition, many other MRSECs have one or more interdisciplinary research group(s) focused on nanoscale science and engineering topics:

- Center for Advanced Materials Research (MRSEC)
  Brown University
- Center for the Science & Engineering of Materials
  California Institute of Technology

- Center for Nanostructured Materials (MRSEC)
  Columbia University
- Center for Materials Research (MRSEC)
  Cornell University
- Center for Materials Science and Engineering (MRSEC)
  Massachusetts Institute of Technology
- Center for Sensor Materials (MRSEC)
  Michigan State University
- Materials Research Science (MRSEC)
  Northwestern University
- Princeton Center for Complex Materials (MRSEC)
  Princeton University
- Center on Polymer Interfaces and Macromolecular Assemblies (MRSEC)
  Stanford University
- Center for Materials for Information Technology (MRSEC)
  University of Alabama
- Center for Materials for Information Technology (MRSEC)
  Materials Research Laboratory
  University of California, Santa Barbara
- Center for Materials for Information Technology (MRSEC)
  Chicago Materials Research Center
  University of Chicago
- Materials Research Science and Engineering Center (MRSEC)
  University of Maryland
- Materials Research Science and Engineering Center on Polymers (MRSEC)
  University of Massachusetts, Amherst
- Materials Research Science and Engineering Center (MRSEC)
  University of Minnesota
- Center for Semiconductor Physics in Nanostructures (MRSEC)
  University of Oklahoma
- The Laboratory for Research on the Structure of Matter (MRSEC)
  University of Pennsylvania
- Center for Nanoscopic Materials Design (MRSEC)
  University of Virginia

6.3.5 (U) NSF Nanoscale Science and Engineering Networks

- Network for Computational Nanotechnology

- National Nanotechnology Infrastructure Network
- Oklahoma Network for Nanostructured Materials
- Nanoscale Informal Science Education Network
- Network for Nanotechnology in Society
  Arizona State University
  University of California-Santa Barbara
- Experimental Program to Stimulate Competitive Research
  University of New Mexico

6.4 (U) Other NNI Institutes and Centers

6.4.1 (U) Department of Defense

- Institute for Soldier Nanotechnologies
  Massachusetts Institute of Technology
- Center for Nanoscience Innovation for Defense
  University of California-Santa Barbara, Riverside and Los Angeles
- Institute for Nanoscience
  Naval Research Laboratory

6.4.2 (U) National Aeronautics and Space Administration (NASA)

6.4.2.1 (U) University Research, Engineering, and Technology Institutes

- NASA Nanotechnology Home Page
- Institute for Intelligent Bio-Nanomaterials & Structures for Aerospace Vehicles
  Texas A&M University
- Biologically Inspired Materials Institute (BIMat)
  Princeton University
- Institute for Nanoelectronics and Computing
  Purdue University

6.4.3 (U) National Institute for Occupational Safety and Health

- Nanotechnology Research Center
  Robert A. Taft Lab

6.4.4 (U) National Institute of Standards and Technology

- Center for Nanoscale Science and Technology
  NIST Gaithersburg

(U) The National Institutes of Health has 21 centers funded as part of the NNI program, but their focus is more biologically oriented so they are not listed here, although there is some overlap between biology and semiconductors in the area of self-assembled materials.

6.5 (U) The Role of Simulation

(U) As the experimental methodologies to synthesize new materials and to characterize them become increasingly sophisticated, the demand for theoretical understanding is driving an ever greater need for materials simulation. This is particularly so in nanoscience, where it is now possible to synthesize a seemingly infinite variety of nanostructured materials and combine them into new devices or systems with complex nanoscale interfaces. The experimental tools of nanoscience—such as scanning probes, neutron scattering, and various electron microscopies—all require modeling to understand what is being measured. Hence, the demand for high-fidelity materials simulation is escalating rapidly, and the tools for verification of such simulations are becoming increasingly available. The World Technology Evaluation Center panel on International Assessment of Research and Development in Simulation-Based Engineering and Science panel on released the following key findings regarding materials simulation[4]:

- Computational materials science and engineering is changing how new materials are discovered, developed, and applied. We are in an extraordinary period in which the convergence of simulation and experiment at the nanoscale is creating new opportunities for materials simulation, both in terms of new targets for study and in terms of opportunities for validation.
- World-class research in all areas of materials simulation areas is to be found in the United States, Europe, and Asia.
  - Algorithm innovation takes place primarily in the United States and Europe, some in Japan, with little activity to date in this area in China.
  - China has been mostly concerned with applications in the past; however, as part of the Chinese government current emphasis on supporting creativity in the both the arts and sciences, one can anticipate increased activity in this area in China.
- There is a rapid ramping-up of materials simulation activities in some countries, particularly China and Germany.
- There is an extraordinary revival of science in Germany, tied to recent increases in the Deutsche Forschungs Gemeinschaft (DFG, German Research Foundation, the equivalent of the U.S. National Science Foundation) budget. In the most recent year, DFG funding jumped over 20%, following on three years of increases in the 5–10% range.

[4] (U) Glotzer, S.C., S.Kim, P.T. Cummings, A. Deshmukh, M. Head-Gordon, G. Karniadakis, L. Petzold, C. Sagui, M. Shinozuka, "WTEC Panel Report on International Assessment of Research and Development in Simulation-Based Engineering and Science," WTEC (22April 2009) [online]

- There is much greater collaboration among groups in code development in Europe compared to the United States. There appear to be several reasons for this:
  - The U.S. tenure process and academic rewards systems mitigate against collaboration.
  - Funding, promotion, and awards favor high-impact science (publications in Nature and Science, for example), while the development of simulation tools is not considered to be high-impact science. There are numerous counter-examples, in which simulation software has been critical in scientific breakthroughs, but typically the breakthrough science comes a long time after a software tool has been developed, adopted widely, and validated. In other words, the payback on the development of a new simulation tool can be a decade or more after it is first developed.
- Training is a critical issue worldwide, as undergraduate students in the physical and chemical sciences and engineering are increasingly illiterate in computer programming. The situation is perhaps most acute of all in the United States.
- Funding of long-term (5 years at the very minimum), multidisciplinary teams is crucial to enable the United States to develop key materials simulation codes that will run on the largest U.S. computing platforms and on future many-core processors. Such codes will be needed to explore the next generation of materials and to interpret experiments on the next generation of scientific instruments.
- The United States is at an increasingly strategic disadvantage with respect to crucial, foundational codes, as it has become increasingly reliant on codes developed by foreign research groups. Political considerations can make those codes effectively unavailable to U.S. researchers, particularly those in Department of Defense laboratories.
- The utility of materials simulation codes for practical application would be enhanced dramatically by the development of standards for interoperability of codes. This would be similar to the CAPE-OPEN effort undertaken in the chemical process simulation (computer-aided process engineering, or CAPE) field to develop interoperability standards in that field (http://www.colan.org).

6.6 (U) Research Journals

(U) The following is a list of research journals[5] provided by NNI, many of which were instrumental in preparing this report. Note that some listings, such as the American Physical Society, contain many additional journals.

- AFRL Nanoscience Technologies Applications, Transitions, & Innovations
- ACS Nano
- Advanced Materials
- American Physical Society journals
- Applied Optics
- Applied Physics Letters

[5] (U) NII list of research journals and other online resources.
http://www.nano.gov/html/research/home_research.html

- AZoNano
- IEEE Transactions on Nanotechnology
- Institute of Nanotechnology
- InterNano
- International Council on Nanotechnology (ICON) and Rice University's Center for Biological and Environmental Nanotechnology (CBEN) online database of scientific findings related to the benefits and risks of nanotechnology
- International Journal of Nanoscience
- The Journal of Nanoparticle Research
- Nanoscience at NSF
- Nanowerk
- NCI Alliance for Nanotechnology in Cancer
- nanoHub
- NanoLetters
- Nanotechnology
- Nanotechweb.org
- Nature
- Nature Nanotechnology
- Proceedings of the National Academy of Sciences
- SciCentral
- Science magazine
- Science Daily
- Small
- Virtual Journal of Nanoscale Science and Technology

(U) Some indications of the amount of scholarly research related to graphene and carbon nanotubes is given in Table 6.1. The Google Scholar hits cover the broadest range of publications, but Google over counts—papers where the key words appear in just citations are counted, so a paper published in 2000 and cited in 2008 and 2007 will generate hits in all three years. Popular papers have a cascading effect causing heavy over counting in more recent years. The number of papers deposited in the preprint server arXiv.org is more representative of condensed matter physics. The number of American Physical Society (APS) sessions held at the annual March meeting is reasonably representative of the popularity of a physics topic. All three measures show a decline for carbon nanotubes and continued growth for graphene. In 2008, eight of the APS sessions had both graphene and carbon nanotubes in the title while there was one joint session in each of the two previous years.

Table 6.1. (U) Research indicators for graphene and carbon nanotubes

Year	Google Scholar Hits		arXiv Papers		APS March Sessions	
	Graphene	Nanotubes	Graphene	Nanotubes	Graphene	Nanotubes
2009					28	10
2008	4,400	18,600	592	215	19	24
2007	3,230	19,700	429	255	8	12
2006	2,350	17,700	176	224	3	26
2005	1,650	15,500	25	225	0	22
2004	1,450	13,500	14	174		14
2003	1,140	10,200	10	124		6
2002	903	7,420	10	144		10
2001	725	5,660	7	77		16
2000	506	3,420	10	64		11

7.0 (U) Conclusions

(U) The fundamental conclusion of this report is that the performance improvements regularly delivered by the semiconductor industry, and represented by Moore's Law, are in no significant danger of disappearing in the near future. The slope of the curve may decline a bit as new technologies transition in, but there are many reasons to believe that challenges the ITRS roadmap currently lists as having no known solution will, in fact, be resolved.

(U) One of the major problems with CMOS is that Dennard scaling has stopped in the face of current losses due to leakage. This affects logic circuits more than memory because the commodity memory industry is more concerned with bulk storage than with speed of access. There is evidence that leakage is less of a problem in carbon-based nanoelectronics, which have superior thermal qualities as well.

(U) Patterning at the nanoscale for commercial devices is a challenge for any technology, silicon or carbon. Lithographic technology as currently practiced, including EUV, may not be adequate to pattern devices at a few nanometers, i.e., order ten atoms. That is not to say that there is no conceivable solution. At least two possibilities present themselves: self-assembly and superlenses. Both of these approaches will require at least a decade of development, perhaps two, before commercially viable systems can be expected.

(U) Moore's Law is only one aspect of building useful devices, however. Maintaining a workable balance among all the components, bandwidth and latency on and off chip as well as amount of storage, is just as big a challenge as cramming more transistors on a chip. Fast processors starved for data don't solve problems. There is reason to believe that integrated optoelectronics will help address some of the bandwidth bottlenecks, but latency is an aspect of physics that simply doesn't scale. Granted, ballistic electrons in graphene or nanotubes do go faster than the ones in silicon, but only by a factor of four. Living with latency is going to demand additional circuit complexity to support deeper pipelines and task programmers to find the concurrency to fill them.

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9.0 (U) IMPLICATIONS

(U//~~FOUO~~) This section of the forecast is added post delivery as reaction from subject matter experts at the National Security Agency as to the implications of the technology and the forecast.

(U//~~FOUO~~) The pace and scope of commercially available electronics used by the USG and society is intricately tied to continued semiconductor technology advancement (Moore's Law). Mission and research investments by the DOD and NSA in advanced electronics are strongly influenced by the expectation of regular improvements along the Moore's Law continuum, which is in transition. Disruptions, modifications, or shifts to this paradigm will have significant impacts on the economy and national security. Understanding the issues influencing this 40+ year trajectory, and identifying potential new directions, is essential if the DOD/NSA is to maintain an asymmetric technology advantage in the future.